# Modelling the OFDM-Based PHY Layer in SoC for Visible Light Communication

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**Abstract—**In this paper, we report a System-on-Chip (SoC) architecture for OFDM-based Visible Light Communication (VLC). The OFDM block was implemented as VLC PHY layer. The OFDM block comprises of transmitter and receiver. In transmitter block, there are Reed-Solomon encoder, modulator, IFFT, and preamble generator. While in receiver block, there are Reed-Solomon decoder, demodulator, FFT, and synchronizer. In SoC, these blocks are designed as IP cores. The industry standard AXI4-Stream protocol was used for data exchange between IP cores. The OFDM model in SoC was verified by comparing with a MATLAB simulation.

**Keywords—**AXI4, OFDM, PHY layer, System-on-Chip, Visible Light Communication

## 1 Introduction

Visible Light Communication (VLC) is an alternative optical-based wireless communication technology, it employs visible light (between Ultraviolet and Infrared spectrums) as its medium. In VLC system, the data is emitted by changing the intensity of an LED. A photodetector (e.g., photodiode, phototransistor, optical camera, light dependent resistor, etc.) is used to detect the transmitted light, it resides at the receiver [1]. VLC offers a solution for energy saving because the lighting and communication functions can be combined in the same device, i.e., LED [2]. There are several digital and analog modulations that can be employed in VLC, the most known modulation used includes OOK, PPM and its variations, PWM and its variations, modulations with OFDM schemes such as BPSK, QPSK, QAM.

Some research has designed prototypes for VLC. In reference [3], a VLC system prototype was implemented in software running on the ARM Cortex-M4 processor. The OFDM modulation was employed in this prototype. In [3], the maximum throughput of 26.8 Kb/s was achieved by using a QPSK modulation scheme. In reference [4], a network-enabled VLC system prototype was carried out in the Zynq-7000 SoC platform. The system consists of peripherals such as USB, Ethernet, etc. The

modulation used in this prototype is digital modulation based on the UART protocol. The system designed in [4] can reach a throughput about 900 Kb/s.

In this short paper, we report an SoC model for OFDM-based VLC system. The model was designed and simulated in Xilinx Zynq-7000 SoC. The main difference between this work to Ref. [3] is the use of DSP as signal processor. In this work, the OFDM model is applied in SoC instead of the general-purposes microcontroller as in [3]. Different from Ref. [4] that uses no modulation scheme (directly fed from UART), we used the OFDM modulation for this work.

This paper correlates with Ref. [5] where the PHY layer of this VLC system is designed as IP cores integrated using the AXI4 system bus. But we more highlight the OFDM model that can be divided into two workloads: OFDM block with customized Xilinx IP cores and OFDM block that are designed from scratch, in which ref. [3] is used as the basis of model. Moreover, due to copyright issues, we only show the OFDM process result at the RTL simulation. The readers can track other research results in [6-8] including modulator and demodulator parts also the overall systems.

## 2 Methods

### 2.1 Review of generic OFDM model

The generic model of the OFDM system is depicted in Fig. 1. On the transmitter side, the bit stream is mapped into symbols by the mapper block. The serial-to-parallel (S/P) block converts the symbols from serial data to parallel data. Let $N_{pilot}$ be the number of pilot data inserted at the output of S/P to construct frequency domain data defined as $X_k$.

The length of this frequency domain data is defined as $N_0$. The IFFT block computes the Inverse Discrete Fourier Transform operation of the $X_k$ to form time-domain data defined as x(n). Define $N_{CP}$ as the number of cyclic prefix (CP) samples inserted at the output of x(n) to form one OFDM data symbol defined as $x_g(n)$, which the dimension is $N_0+N_{CP}$.

The cyclic prefix is used to overcome the Inter Symbol Interference (ISI) problem. The parallel-to-serial (P/S) block converts the $x_g(n)$ from parallel data to serial data. The D/A converts the digital data to analog data; then it is transmitted through the channel $h(n)$ and AWGN $z(n)$.

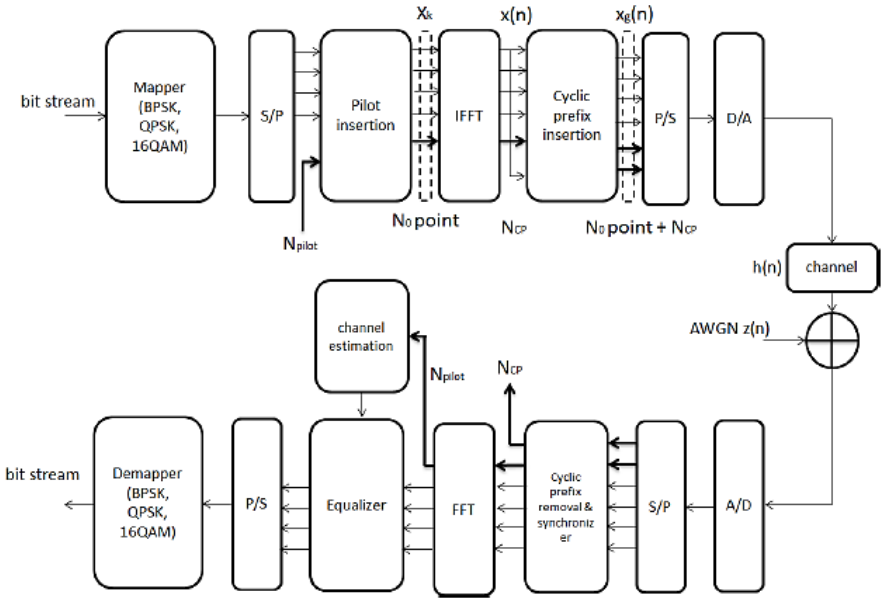


**Fig. 1.** The generic model of the OFDM system

On the receiver side, the A/D samples the OFDM signal; then it is converted to digital data. The serial-to-parallel (S/P) block converts the serial data to parallel data. The synchronization proses find the start of the OFDM data symbol. The NCP cyclic prefix samples need to be removed from the synchronized OFDM data. The FFT computes the time domain data to get back the frequency domain data. The channel estimation block estimates the channel response based on the pilot data. The equalizer block equalizes the distorted OFDM data by using the expected channel frequency response. The parallel-to-serial (P/S) block converts the parallel data to serial data. This serial data are the symbols that are ready to be de-mapped by the de-mapper block. The final output is the bit stream data.

FFT and IFFT are the main components of the OFDM systems. These blocks are mainly complex-valued. In RF systems, the complex-valued numbers are converted to real-valued by the up-converter block. This block is used to upconvert the frequency of a baseband signal to the frequency of the regulated carrier (bandpass signal). In VLC systems, there is no carrier signal. The up conversion is not necessary because of these several factors: the VLC spectrum is not regulated, the complexity of the circuit, and the limited bandwidth of the LED and photodiode [3].

In VLC systems, the output of IFFT and the input of FFT are needed to be re-al-valued. This real-valued baseband signal can be sent with LED and received with a photodiode. To remove the imaginary value of the complex number in the FFT and IFFT process, we use the Hermitian symmetry, so the output of IFFT and the input of FFT are real-valued. It exploits the DFT property, namely the DFT of a real-valued signal has Hermitian symmetry, i.e., the DFT result is mirrored (symmetric complex conjugate) between the positive and negative frequency. On the IFFT side, the IFFT's

input data need to be symmetric complex conjugate, so the transmitted OFDM signal is real-valued.

For applying the Hermitian symmetry on OFDM system, the data symbols need to be modified as in Ref. [3]. Let $N_{DFT}$ be the length of the IDFT input X[k] on the transmitter. Define half of the DFT length as $N_{DFT}/2$. Let $N_{DFT}/2$ be the number of data symbols from mapper block, and the other half $N_{DFT/2}$ be the number of complex conjugate of the $N_{DFT}/2$ data symbols, so the X[k] is defined from frequency $0 \leq k \leq N_{DFT}$-1 as

$$X[k] = (X[0], \dots, X\left[\frac{N_{DFT}}{2} - 1\right], X^*\left[\frac{N_{DFT}}{2} - 1\right], \dots, X^*[0]) \quad (1)$$

where X [0] to X[$N_{DFT}$/2-1] is the data symbols. Then, apply the IDFT operation to X[k] to obtain the result x[n], that is given from time $0 \leq n \leq N$-1 as

$$x[n] = \frac{1}{N}\sum_{k=0}^{N-1} X[k]e^{j2\pi kn/N} \quad (2)$$

The x[n] is real-valued, i.e., the imaginary value is zero. On the receiver, apply the DFT operation to obtain back the X[K], given as

$$X[K] = \sum_{k=0}^{N-1} x[n]e^{-j2\pi kn/N} \quad (3)$$

Take X[k], where $0 \leq k \leq N_{DFT}/2$-1, to obtain the data symbols. The X[k], where $N_{DFT}/2 \leq k \leq N_{DFT}$-1 can be ignored because they are just the redundancies of the data symbols.

This model is used in Ref. [9] [10], but only simulated in MATLAB. While in Ref. [3], the model, as depicted in Fig. 1 has been implemented as a real-time VLC system based on microcontroller. In this paper, we model the generic OFDM block as in Fig. 1 to SoC design with reuse methodology.

### 2.2 VLC PHY block diagram

The VLC PHY block diagram is depicted in Fig. 2. The black-colored blocks are the customized Xilinx IP cores, while the white-colored blocks are the IP cores designed from the scratch. The transmitter and receiver control blocks are the memory-mapped controllers. These blocks are connected to the processor through the AXI4 system bus and are also used for converting the memory-mapped data to the stream data, because the protocol used in the next blocks is AXI4-Steam (AXIS). In the transmitter, there are Reed-Solomon encoder, OFDM framing, modulator, IFFT, and preamble generator. The output data from the preamble generator block will be sent to the DAC. In the receiver, there are Reed-Solomon (RS) decoder, OFDM deframing, demodulator, FFT, and synchronizer. The input data for the synchronizer comes from the ADC.

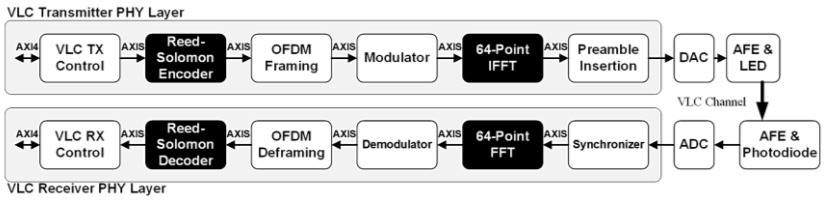


**Fig. 2.** VLC PHY block diagram

### 2.3 RS encoder and decoder

The RS was used as the Forward Error Correction (FEC) in this PHY. The RS code for this PHY consists of 73 data symbol and 32 parity symbol, that is RS(105,73). Accordingly, the total symbols are 105 symbols in which the symbol size is 8-bit.

### 2.4 Modulator and demodulator

Three modulation/mapper schemes can be selected in this PHY layer, namely, BPSK, QPSK, and 16-QAM. In BPSK modulation, every 1-bit of data is a BPSK symbol [11-12]. In QPSK modulation, every 2-bits of data is a QPSK symbol [13]. In 16-QAM modulation every 4-bits of data is a 16-QAM symbol [14].

### 2.5 IFFT and FFT

The IFFT was used for transforming the subcarriers data, i.e., the group of BPSK, QPSK, or QAM-16 symbols to the time-domain whereas the FFT was used for processing the time-domain data back to the subcarriers data. The IFFT and FFT length is 64-point, so there are 64 subcarriers, as shown in Fig. 3.

Subcarriers $X_0$ and $X_{32}$ are filled with 0. Subcarriers $X_{33}$ to $X_{63}$ are the complex conjugate of subcarriers $X_1$ to $X_{31}$ to achieve the Hermitian symmetry. In OFDM for VLC, the output of the IFFT must be real and positive numbers. This condition is required because, in VLC, there is no up-conversion process that combines the real and imaginary part [3], [15]. In OFDM for VLC, the real and positive output can be realized by imposing Hermitian symmetry in the frequency domain [16]. A sample of one OFDM symbol in time-domain can be seen in Fig. 4.

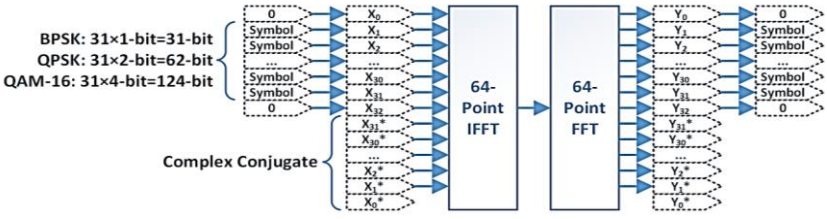


**Fig. 3.** FFT and IFFT subcarriers

The subcarriers X1 to X31 can be filled with the BPSK, QPSK, or 16-QAM symbols. The maximum payload for BPSK, QPSK, and 16-QAM in one OFDM symbol is 31-bit, 62-bit, and 124-bit, respectively.

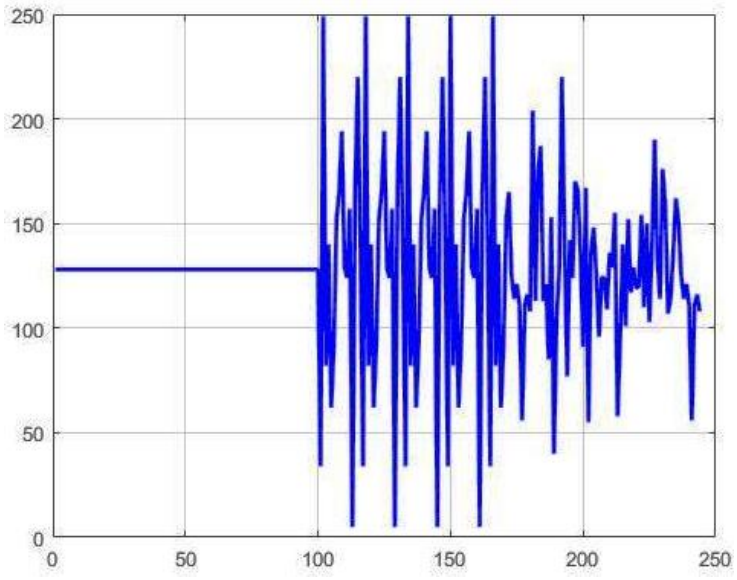


**Fig. 4.** The appearance of one OFDM symbol

### 2.6 Preamble and synchronizer

Preamble generator block was used for adding preamble structure before the data. This preamble is used for detecting the beginning of the OFDM symbol at the receiver. The preamble and the data of one OFDM symbol is depicted in Fig. 4. The CP is added to the beginning of both preamble and data. The CP ratio is 1/8, so the total sample for one OFDM symbol is 144 samples. The synchronizer block is used for detecting the beginning of the data. Cross-correlation operation is used in this synchronizer. This operation calculates the similarity between preamble in input signal and preamble stored in the receiver. If both of the preambles coincide, then the output of the process has four peaks. If this pattern occurs, then there is an OFDM symbol being transmitted.

### 2.7 OFDM framing and deframing

OFDM framing block was used for dividing the RS code to several OFDM symbols because the RS code size is 105 bytes, but the maximum payload for one OFDM symbol is 15 bytes (with QAM-16). OFDM deframing was used for combining the OFDM symbols back to RS code.

# 3 Results

As introduced in the first section, we perform on the RTL test only. The RTL test consists of two parts: RTL simulation using the Vivado simulator to obtain information such as latency and throughput of VLC PHY based on OFDM. The second test is verification of FPGA implementation, we can verify the OFDM signal by using an oscilloscope. In this work, we focus on first scenario as presented in Section 3.1 while the FPGA implementation is explained in Ref. [5].

## 3.1 RTL simulation

Functional verification of the RTL design is done by connecting the transmitter and receiver in loopback configuration. After that, the payload data, which the size is 124-bits (divided into 4 words) is transmitted. Fig. 5 shows the transmitted data, while Fig. 6 shows the received data. The received data is compared with the transmitted data. Once the RTL simulation has been done carefully, we test the transmitter and receiver timing diagram as presented in Section 3.2 and 3.3 respectively.

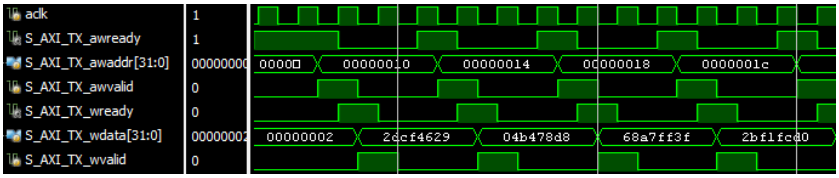


**Fig. 5.** The transmitted OFDM payload (one data symbol)

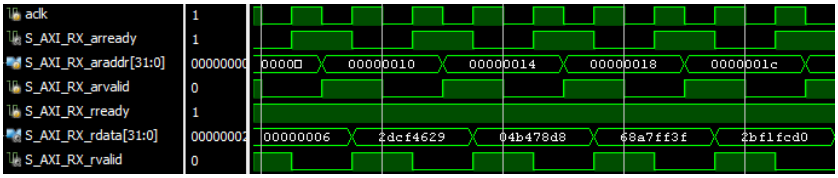


**Fig. 6.** The received OFDM payload (one data symbol)

## 3.2 VLC Transmitter timing diagram

VLC transmitter timing diagram is shown in Fig. 7. In this diagram, there is a start, busy, done, and data signals. The start signal is generated by the controller for one clock cycle after the processor writes the last data to the data register. The busy signal is set to logic one when the start signal is generated. The done signal is generated for one clock cycle after the OFDM signal transmission is completed. The busy signal is cleared to logic zero when the done signal is generated. The processor can read the busy signal in the control register, so the software will not send new data before the first data is sent. The computation time in VLC transmitter is the time between start tick until the data is sent to the output (DAC).

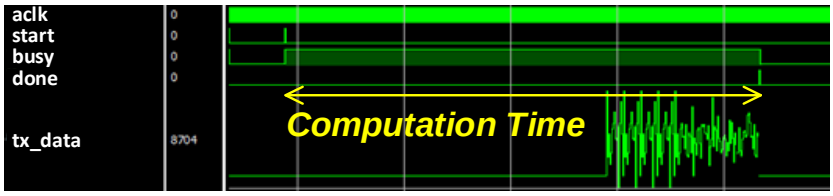


**Fig. 7.** VLC transmitter timing diagram

### 3.3 VLC Receiver timing diagram

VLC receiver timing diagram is shown in Fig. 8. In this timing diagram, there is a trigger, ready, done, and data signals. The synchronizer generates the trigger signal for one clock cycle after the start of the OFDM data symbol is detected. The ready signal is set to logic one when the data is prepared to be read by the processor. This available signal will be cleared to logic zero when the data has been read by the processor, which is indicated by the done signal. The computation time in VLC receiver is the time between the first received data until the ready tick has occurred.

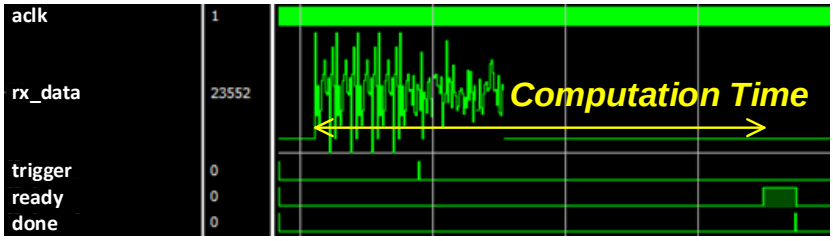


**Fig. 8.** Receiver timing diagram

### 3.4 Throughput and latency analysis

The computation time is obtained from the timing diagram. The clock speed of the simulation is 100 MHz. The computation time for modulating one OFDM symbol (124-bit payload) is 4.46 μs, while the computation time for demodulating one OFDM symbol (124-bit payload) is 3.38 μs. The net data rate of the simulated OFDM system is given as

$$Net\ Data\ Rate_{sim} = \frac{1}{Computation\ Time_{sim}}.124 \tag{4}$$

where 124 is the number of payload bits of one OFDM symbols. The net data rate of the simulated 16-QAM, QPSK, and BPSK OFDM system are 26.51 Mbit/s, 13.31 Mbit/s, 6.67 Mbit/s respectively.

The latency of each PHY OFDM block is as follows: Synchronizer, Preamble generator, FFT, IFFT, QAM-16 demodulator, QAM-16 modulator, QPSK demodulator,

QPSK modulator, BPSK demodulator, BPSK modulator, RS decoder, and RS encoder, i.e., 80, 72, 190, 193, 65, 34, 65, 32, 65, 31, 686, 5 respectively.

## 4 Conclusion

The OFDM design based on SoC architecture for VLC system is presented in this paper in which the OFDM block is implemented for VLC PHY layer. According to the simulation, the OFDM can be run in MATLAB and RTL as well. A maximum simulated net data rate of 26.51 Mbit/s and minimum at 6.67 Mbit/s using 100 MHz clock are achieved using this OFDM model.

## 5 Acknowledgement

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