Wideband 5-bit MMIC Digital Attenuator With High Precision

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***Abstract*—This paper mainly introduces the Wideband 5-bit MMIC digital attenuator with high precision. Firstly, the theories of basic GaAs digital attenuator MMIC's configurations are searched. Secondly, every possible configuration is contrasted, subsequently, appropriate topology is selected for each stage. This attenuator has been realized by 0.5μm GaAs pHEMT process. Simulation results of the digital attenuator has 0.25dB resolution and 7.75dB dynamic attenuation range, Input Voltage Standing Wave Ratio($VSWR_{IN}$) was less than 1.55 and Output Voltage Standing Wave Ratio($VSWR_{OUT}$) was less than 1.6 for all attenuation states, high attenuation accuracy is less than ±0.26dB; insertion loss is less than 1.3dB; The layout of the digital attenuator with a chip size is 0.93 mm×1.45 mm**

***Index Terms*—wideband, 5-bit, digital attenuator, high precision**

I. INTRODUCTION

MMIC variable attenuators are required in many microwave systems for automatic gain control for receiver and transmitter systems, amplitude weighting for phased array radars and temperature compensation of microwave amplifiers. An attenuator specially is a key device of the module used in BFN because the attenuator is to control of the amplitude[1~4].

The attenuator has two types of control method, analog attenuator and digital attenuator. Digital attenuators offer better linearity, high power handling, and easy and accurate control of attenuation, So MMIC digital attenuators have gained lots of interest in recent years[5~6].

The requirements of the MMIC digital attenuators to be designed are as following: small size, high attenuation accuracy, low insertion phase shift, high reliability and low cost[7].

In this paper, we describes an Wideband 5-bit MMIC digital attenuator with high precision. The digital attenuator has obtained excellent performances and implements in 0.5um GaAs pHEMT MMIC.

II. CIRCUIT DESIGN

Published literature on MMIC digital attenuators mainly rely on three basic types of topologies: i) Tee attenuator; ii) Bridged-Tee attenuator; iii)Pi attenuator. All of them relay on a signal through either a bypass line or an attenuation cell with RF switches. Fig.1, Fig.2 and Fig.3 show the topologies of Tee attenuator, Bridged-Tee attenuator and Pi attenuator[8~11].

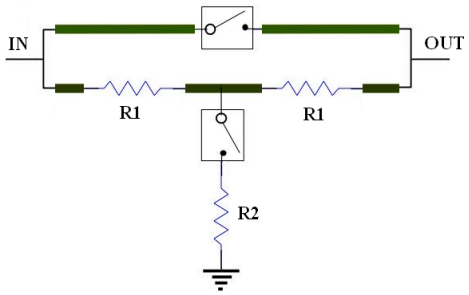

Figure 1. Tee attenuator

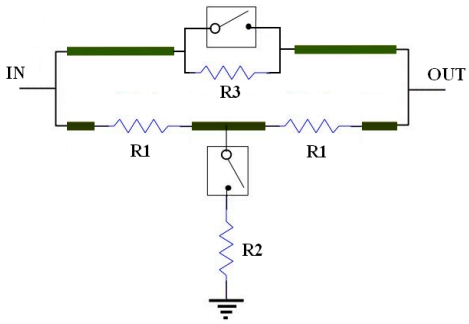

Figure 2. Bridged-Tee attenuator

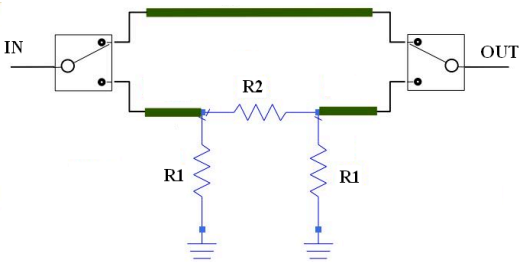

Figure 3. Pi attenuator

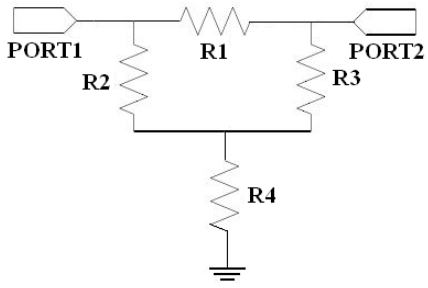

Figure 4. The equivalent circuit of Bridged-Tee attenuator

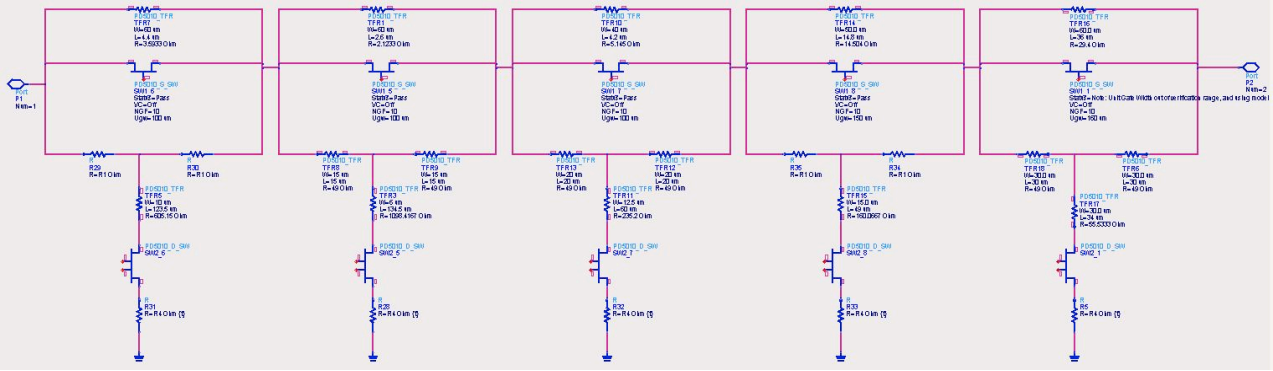

Figure 5. Mainly schematic of the digital attenuator

Referring to FIG.5. the schematic of the x-band MMIC digital attenuator with low phase shift is shown. To achieve good performance, the circuit configuration as well as the process conditions, should be selected properly.

The digital attenuator consists of switched pHEMTs, resistors, and microstrip lines. The switched PHEMTs in the circuit are controlled through 8kΩ resistors of the gate poles, which provide enough radio frequency isolation between the gate of each switched PHEMT and the control sources. And the low value resistors are used to form the topologies for attenuators[12~14].

The five required attenuation bits are the 0.25dB, 0.5dB, 1dB, 2dB and 4dB, providing a dynamic range from 0.25dB to 7.75dB. the most attenuation of five mainly attenuation states is 4dB, Bridged-Tee attenuator are used for the Wideband 5-bit MMIC digital attenuator. Bridged-Tee attenuator (Fig.2) has good performance in insertion loss, $VSWR_{IN}$ and $VSWR_{OUT}$ also has better performance than Pi attenuator[15~17].

Referring to Fig.4, The equivalent circuit of Bridged-Tee attenuator shows (R_2=R_3):

$$Z=\begin{bmatrix}\frac{R_1Z_0}{R_1+2Z_0}+R_4 & \frac{Z_0^2}{R_1+2Z_0}+R_4\\ \frac{Z_0^2}{R_1+2Z_0}+R_4 & \frac{R_1Z_0+Z_0^2}{R_1+2Z_0}+R_4\end{bmatrix}=\begin{bmatrix}Z_{11} & Z_{12}\\ Z_{21} & Z_{22}\end{bmatrix} \quad (1)$$

The characteristic impedance of transfers lines connect to port1 and port2 are Z_{in} and Z_{out}, so:

$$Z=\begin{bmatrix}\frac{Z_{11}}{Z_{in}} & \frac{Z_{12}}{\sqrt{Z_{in}+Z_{out}}}\\ \frac{Z_{21}}{Z_{in}\cdot Z_{out}} & \frac{Z_{22}}{Z_{out}}\end{bmatrix}=\begin{bmatrix}Z_{11} & Z_{12}\\ Z_{21} & Z_{22}\end{bmatrix} \quad (2)$$

The S-parameters are:

$$S_{11}=\frac{|Z|-1+Z_{11}-Z_{22}}{|Z|+1+Z_{11}+Z_{22}} \quad (3)$$

$$S_{22}=\frac{|Z|-1-Z_{11}+Z_{22}}{|Z|+1+Z_{11}+Z_{22}} \quad (4)$$

$$S_{21}=\frac{2Z_{21}}{|Z|+1+Z_{11}+Z_{22}} \quad (5)$$

$$S_{12}=\frac{2Z_{12}}{|Z|+1+Z_{11}+Z_{22}} \quad (6)$$

And:

$$L=20\lg|S_{21}| \quad (7)$$

$$10\lg|S_{11}|=-\infty \quad (8)$$

From (1)~(8),the value of R_1 and R_4 in Bridged-Tee attenuator can show below:

$$R_1=Z_0\left(10^{\frac{L}{20}}-1\right) \quad (9)$$

$$R_4=\frac{Z_0}{10^{\frac{L}{20}}-1} \quad (10)$$

From (9)~(10), the value of R_1 and R_4 can be calculated by given attenuation bits.

The digital attenuator integrated driver was realized by enhancement /depletion (E/D) technology on GaAs substrate. The digital portion adopts a direct coupled FET logic (DCFL) structure, which had the advantages of simple structure, high speed, low power consumption. simplify the system application and enhances the system reliability. The digital attenuator has built-in 5 voltage control port transistor-transistor logic (TTL) driving circuit to feed the pHEMTs' gate poles. In this case, when the control voltages are set at 0V, which is the negative pinch-off voltage of switched pHEMT, the switched pHEMT will work at its "off" state (high resistance). When the control voltages are set at 5V, The switched pHEMT will work at its "on" state. So the required attenuation can be obtained by switching the control voltages at the port.

The digital attenuator is at the minimum attenuation state, when all of the five control voltages are 5 V. In this case, the attenuator has a minimum insertion loss. The attenuator is at the maximum attenuation state, when all of the five control voltages are 0 V.

The above description is equally available for the other states. The control signal with the value of 0 V is taken as "0" and the control signal with the value of 5 V is taken as "1." The truth table of the digitally-controlled main attenuation states shows in Table 1, which is referred to in Fig. 6.

TABLE I.
TRUTH TABLE OF MAIN ATTENUATION STATES SHOWS
("1"AS 0V, "0"AS -5V)

	0.25dB	0.5dB	1dB	2dB	4dB
	P1	P2	P3	P4	P5
MIN	1	1	1	1	1
0.25dB	0	1	1	1	1
0.5 dB	1	0	1	1	1
1 dB	1	1	0	1	1
2 dB	1	1	1	0	1
4 dB	1	1	1	1	0
MAX	1	1	1	1	1

The layout of the Wideband 5-bit MMIC digital attenuator with high precision as shown in Fig.6. RF input and output are at the either end with complementary pairs of the control lines along one edge, control lines the other edge are all connect to GND. The layout of the digital attenuator with a chip size is 0.93 mm×1.45 mm.

III. SIMULATED RESULTS

Using the new configuration, a digital attenuator has been realized by 0.5um GaAs E/D process. The simulation of our digital attenuator have been presented based on the ADS2008.Broadband and high precision performance was achieved by optimization of the transmission line parameters and the resistor values. The Monte Carlo analysis were also utilized in the attenuator design, the results predicted that the design has stability against the process variations.

The insertion loss is shown in Fig.7. The attenuator achieved a minimum insertion loss of 0.5~1.3dB in the entire DC~4GHz band. Referring to Fig.8, It can be seen that each curve in the figure represents a different attenuation setting in a roughly 0.25dB step with over 7.75dB dynamic range, for which a proper combination of the control voltages was chosen. Fig.9 and Fig.10 show $VSWR_{IN}$ and $VSWR_{OUT}$ for 35 attenuation states. The $VSWR_{IN}$ was always less than 1.55 and the $VSWR_{OUT}$ was always less than 1.6 at any attenuation setting, the attenuation accuracy is less than ±0.26dB;

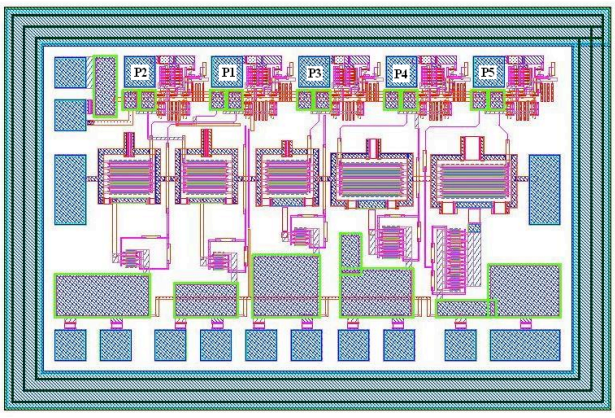

Figure 6. The layout of Wideband 5-bit MMIC digital attenuator with high precision

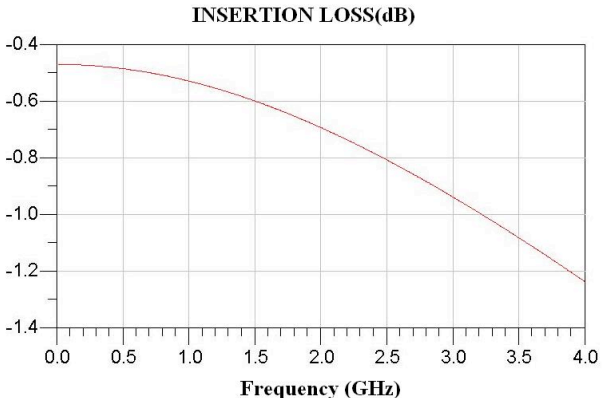

Figure 7. Insertion Loss

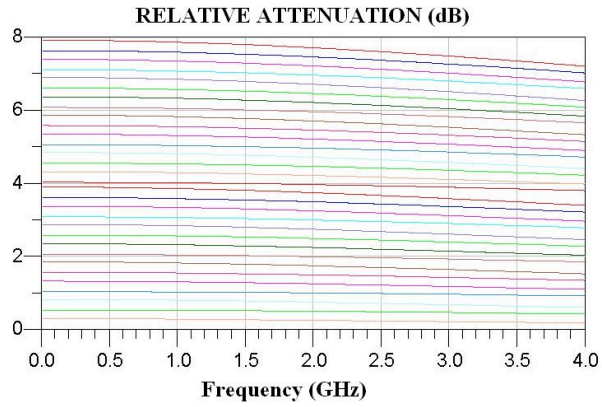

Figure 8. Relative Attenuation

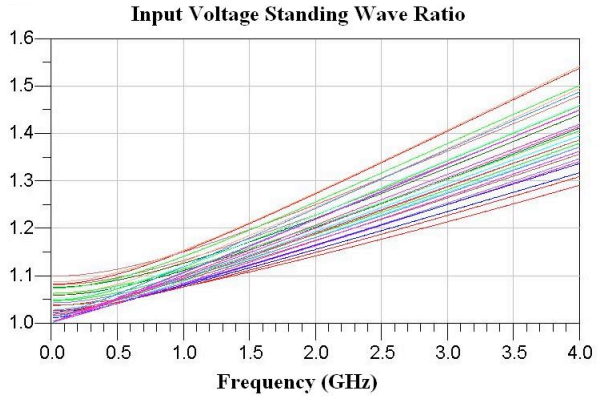

Figure 9. Input Voltage Standing Wave Ratio

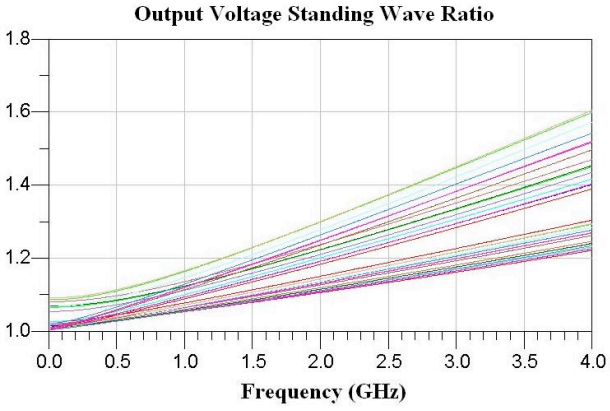

Figure 10. Output Voltage Standing Wave Ratio

IV. CONCLUSION

The theory, design, and measurement of the Wideband 5-bit MMIC digital attenuator with high precision are presented. appropriate topology is selected for stages. To ensure high yield, Performance redundancy optimization strategy is used in design. the simulation results of the developed MMIC chips show that the 5-bit MMIC digital attenuator has 0.25dB resolution and 7.75dB dynamic attenuation range, $VSWR_{IN}$ was less than 1.55 and the $VSWR_{OUT}$ was less than 1.6 for all attenuation states; insertion loss is less than 1.3dB; attenuation accuracy is less than ±0.26dB for all 35 attenuation states. The MMIC chip size is 0.93 mm×1.45 mm. This proposed MMIC has shown excellent performance covering DC~4GHz for digital attenuator.

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