Design and Analysis of High Frame Rate Capable Active Pixel Sensor by Using CNTFET Devices for Nanoelectronics

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***Abstract*—This paper presents a high frame rate capable Active Pixel Sensor (APS) using Carbon Nanotube Field Effect Transistor (CNTFET) instead of Complementary Metal Oxide Semiconductor (CMOS). Conventionally, the design of a single APS circuit is based on three transistors (3T) model. In order to achieve higher frame rate, one extra transistor with a column sensor circuit has been introduced in the proposed design to reduce the readout time. This study also concerns about the effect of transistor sizing, bias current, and moreover, the chiral vector of CNTFET. The power consumption and power delay product (PDP) are also investigated for specific sets of reset and row selector signal. Data for these studies were collected with the help of HSPICE software which were further plotted in OriginPro to analyze the optimal operation point of APS circuit. The bias current was also recorded for the readout transistor which is uniquely introduced in the proposed model for achieving better readout time. Hence, the main focus of this paper is to improve the frame rate by reducing the readout time. Results of the proposed CNTFET APS circuit are compared with the conventional CMOS APS circuit. The performance benchmarking shows that CNTFET APS cell significantly reduces readout time, PDP, and thus can achieve much higher frame rate than that of conventional CMOS APS cell.**

***Index Terms*— Active Pixel Sensor (APS); Carbon Nanotube Field Effect Transistor (CNTFET); Complementary Metal Oxide Semiconductor (CMOS); Chiral vector.**

I. INTRODUCTION

An Active Pixel Sensor (APS) is an image sensor consisting of an integrated circuit containing an array of pixel sensors, each pixel containing a photo detector and an active amplifier. Different kinds of Sensors are designed based on Active Pixel Sensor such as CMOS APS most commonly used in digital cameras, web cameras, DSLRs, NMOS process and Charge Couple Device (CCD) image sensor. APS converts optical information to electrical signal. This conversion is done by a photodiode. Basically, CMOS APS uses a three-transistor APS pixel and column APS circuit [1]. Now a days CMOS active pixel sensor is commercially available and the frame rate of that sensor is higher than Charge Couple Device (CCD). In this paper a Carbon Nanotube Field Effect Transistor (CNTFET) active pixel sensor has been designed by using a unique readout time reduction technique. CNTFET is most recent technology which is invented in 1998. It has high performance due to ballistic transfer of electrons and other beneficial properties of CNTFET are high mobility, compatibility, low-leakage current and low power consumption [2]. In proposed circuit one extra transistor has been introduced to reduce the readout time. Shorter readout time can be achieved by reducing bias current and hence reduces energy consumption. This study shows that frame rate can be improved using CNTFET instead of CMOS. In CNTFET based proposed design one extra transistor is used with parallel to output capacitor (C_o). This transistor has been used to discharge the output capacitate voltage when a sample is readout so that again the circuit is able to read a new sample. Optimization was done for this APS circuit due to dependency of parameters to each other.

This paper is organized as follows: CNTFET device overview is discussed in section II. Section III describes the device simulation of CNTFET. CMOS vs CNTFET performance analysis is discussed in section VI. Section V describes 3T active pixel sensor (APS) overview. In section VI, it elaborates the high frame rate capable APS design and its optimization. Performance analysis of the proposed APS has been comprehended in section VII. In section VIII, finally the paper ends with a conclusion. The paper provides substantial advantages in terms of PDP, reduced readout time rate, and chip area when CNTFETs are employed in the proposed design.

II. CNTFET DEVICE REVIEW

Carbon Nanotube (CNT) is a Nano-scale tube created as a rolled sheet of graphite which was discovered in 1991 by Dr. Iijima [3]. A CNT can be multi-wall (MWCNT) or single-wall (SWCNT) [4]. A MWCNT consists of more than one cylinder whereas a SWCNT is a single cylinder. The diameter of SWCNT can be as small as 0.4nm [5]. The following relation expresses the SWCNT band gap energy.

$$E_{gap} = \frac{2\gamma_o a_{c-c}}{d} \quad (1)$$

Where E_{gap} is the band gap, γ_o is the carbon-to-carbon tight-binding overlap energy, a_{c-c} is the nearest neighbor carbon-to-carbon distance (0.142 nm), and d is the diameter of the nanotube. A chiral vector C_h is the vector perpendicular to the tube axis T, given by

$$\overline{C_h} = n\overline{a_1} + m\overline{a_2} \quad (2)$$

CNTFET is represented by two pair of integer m and n. The equation for calculating the diameter is given below [6].

$$D_{CNT} = \frac{a_o\sqrt{3}}{\pi}\sqrt{(m^2 + mn + n^2)} \quad (3)$$

Where, a_o =0.142nm is the inter-atomic distance between each carbon atom and its neighbor. CNTFET device can be electrostatically turned on or off via the gate. As the chirality vector changes, the threshold voltage of the CNTFET will also change.

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \quad (4)$$

Where, a = 2.49 Å is the carbon to carbon atom distance, V_π = 3.033 eV is the carbon π–π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter. In the proposed design the threshold voltage of NCNTFET using (19, 0) CNTs as channels is 0.2931V calculated from (3), (4) and D_{CNT} of (19, 0) CNTs is only 1.487 nm. Fig. 1, shows the construction of a graphene sheet.

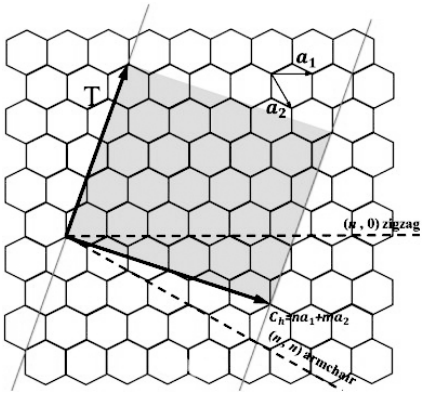

Figure 1. Construction of graphene sheet and important parameters for CNTs (C_h is chiral vector) [6]

The I-V characteristic of the CNTFET is shown in Fig. 2. The characteristic curve is similar to that of MOSFET. The calculated threshold voltage, V_{th} for (5, 0) CNTs is 1.0982V.

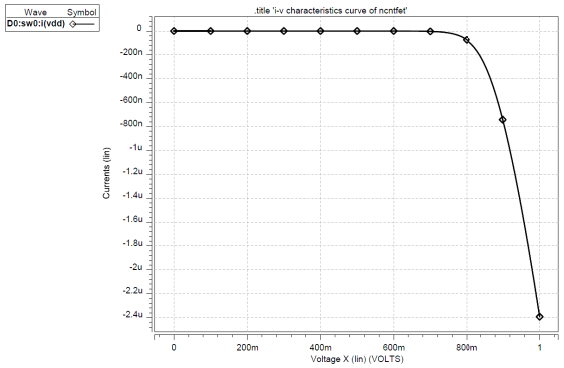

Figure 2. I–V characteristics curve of a typical NCNTFET (22nm) for the chirality vector (5, 0)

The characteristic curve is similar to that of MOSFET. The CNTFET device current is saturated at higher V_{ds} (drain to source voltage), as channel length increases the ON-current decreases due to energy quantization in the axial direction at a lower gate length of CNTFETs.

III. DEVICE SIMULATION OF CNTFET

An equivalent circuit model for the channel region of basic CNTFET is given in Fig. 3. The three current sources considered in this CNTFET model: (i) the thermionic current contributed by the semiconducting sub-bands *(I_{semi})* with the classical band theory, (ii) the current contributed by the metallic sub-bands *(I_{metal})*, and (iii) the leakage current *(I_{btbt})* caused by the band to band tunneling (BTBT) mechanism through the semiconducting sub-bands [6]. The thermionic current contributed by the semi conducting sub-bands is given by

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) \approx \frac{4e^2}{h}\sum_{k_m,m=1}^{M} T_m \cdot \left[V_{ch,DS} + \frac{kT}{e} ln\left(\frac{1+e^{(E_{m,0}-\Delta\phi_B)/kT}}{1+e^{(E_{m,0}-\Delta\phi_B+eV_{ch,DS})/kT}}\right)\right] \quad (5)$$

where, $V_{ch,DS}$ and $V_{ch,GS}$ denotes the Fermi potential differences near source side within the channel, e is the unit electrical charge, $\Delta\phi_B$ is the channel surface potential charge with gate/drain bias, T_m is the transmission probably, k is the Boltzmann constant, T is the temperature in Kelvin and $E_{m,0}$ is the half band gap of the *m-th* sub-band. In the sub-threshold region, especially with negative gate bias (nFET), the band-to-band tunneling current from drain to source becomes significant. For metallic sub-bands of metallic nanotubes, the current includes both the electron and hole currents [6]. The simplified equation for I_{metal} is given by

$$I_{metal} = 2(1 - m0)\frac{4e^2}{h}T_{metal}V_{ch,DS} \quad (6)$$

where, T_{metal} is transmission probability. The above equation shows that I_{metal} is independent of the channel surface-potential change $\Delta\phi_B$ as expected because the density of states (DOS) of metallic CNT is independent of the carrier energy. A voltage controlled current source I_{btbt} is included in the device model in order to evaluate the device sub-threshold behavior and the static power consumption [6]. The expression for I_{btbt} is given by

$$I_{btbt} = \frac{4e}{h}kT.\sum_{k_m,m=1}^{M}\left[T_{btbt} ln\left(\frac{1+e^{(eV_{ch,DS}-E_{m,0}-E_f)/kT}}{1+e^{(E_{m,0}-E_f)/kT}}\right)\times \frac{max(eV_{ch,DS}-2E_{m,0},0)}{eV_{ch,DS}-2E_{m,0}}\right] \quad (7)$$

where, E_f is the Fermi level of the doped source/drain nanotube in electron-volt unit. T_{btbt} is the Wentzel–Kramers–Brillouin-like transmission coefficient. To model the intrinsic ac response of CNTFET device, a controlled trans-capacitance array among the four electrodes (Gate, Drain, Source, and Substrate) with the Meyer capacitor model has been used [6]. Thereby, the equations for capacitance calculation are given below

$$C_{gs} = \frac{L_g C_{ox}[C_{Qs}+(1-\beta)C_c]}{C_{tot}+C_{Qs}+C_{Qd}} \quad (8)$$

$$C_{gb} = \frac{L_g C_{ox}(C_{Qd}+\beta C_c)}{C_{tot}+C_Q+C_{Qd}} \quad (9)$$

$$C_{bs} = C_{gs}\frac{C_{sub}}{C_{ox}} \quad (10)$$

$$C_{bd} = C_{gd}\frac{C_{sub}}{C_{ox}} \quad (11)$$

In this paper, all circuits have been simulated in HSPICE. A 22nm process has been used for designing purpose. The CNFET model files are taken from Stanford University [7].

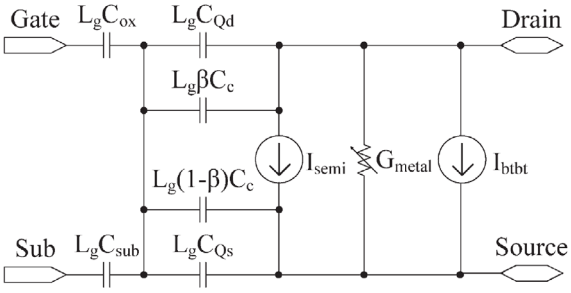

Figure 3. Equivalent circuit model for intrinsic channel region of a CNTFET [6]

The model files for CMOS (incorporated high-κ/metal gate and stress effect) are taken from Predict Technology Model (PTM) of Arizona State University [8].

IV. CMOS VS. CNTFET PERFORMANCE ANALYSIS

The total power dissipation can be found as a summation of dynamic power dissipation and static (leakage) power dissipation which can be given by

$$P_{total} = P_{dynamic} + P_{static} \quad (12)$$

A. Analysis of CMOS inverter under 22nm technology

Considering impeccable fabrication, P_{static} becomes negligible. To be noted that power dissipated as gate leakage was found to be about 10% of P_{static} for CMOS gates and less than 1% of P_{static} for CNTFET because of the high-κ dielectric used as gate insulator in CNTFETs [7]. DC characteristic curve for CMOS inverter is shown in Fig. 4.

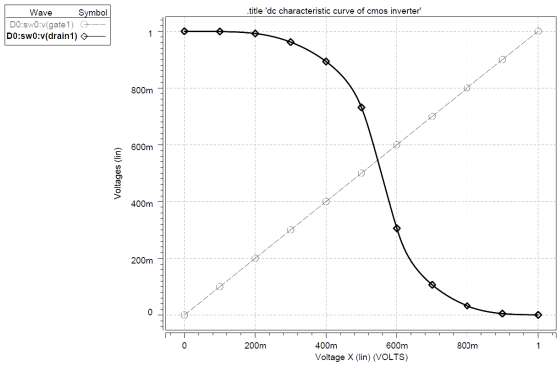

Figure 4. DC analysis of CMOS inverter (22nm)

B. Analysis of CNTFET inverter under 22nm technology

The logic gates in the generalized CNTFET library dissipate 28% less power on average than a library of conventional CMOS gates [9]. The Fig. 5, shows the DC characteristic curve of CNTFET inverter.

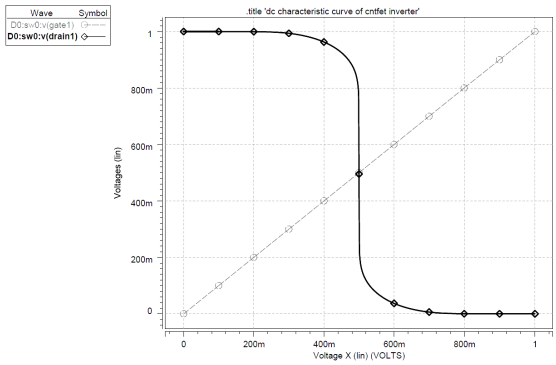

Figure 5. DC analysis of CNTFET inverter (22nm)

In both Fig. 4 and Fig. 5, step by step the gate voltage is increased to 1V. At $V_g=0V$ then V_o is high, and while at $V_g=1V$ then V_o is low. Of these two DC characteristic curves the inversion slope of CNTFET is steeper. From the following Table I it has been calculated that CNTFET inverter dissipates 98.23% less dynamic power and operates 50.07% faster than that of CMOS inverter. To be noted that the data is Table I are attained from HSPICE simulation of CNTFET and CMOS inverter.

TABLE I.
ENERGY CONSUMPTION TABLE

Description	Dynamic Power, $P_{dynamic}$ (W)	Delay, t_d (Sec)	PDP (J)
CNTFET	2.3912e-09	4.2542e-12	1.0172e-20
CMOS	1.3544e-07	8.3872e-12	1.1359e-18

V. 3T ACTIVE PIXEL SENSOR (APS) OVERVIEW

Active pixel sensor converts optical information to electrical signal by using photodiode. Photodiode is normally a p-n junction. It operates in reverse bias. Active pixel basically has three transistors in a single pixel circuit. Fig. 6 shows a conventional 3T based CMOS APS.

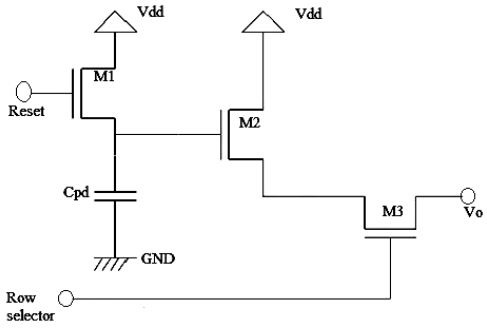

Figure 6. Conventional 3T based CMOS APS cell

In HSPICE simulation C_{pd} is regarded as equivalent to photodiode capacitance. M_1 is the reset transistor and M_2 is source follower. M_3 is the row selector transistor which is active when a sample is being read.

VI. HIGH FRAME RATE CAPABLE APS DESIGN AND ITS OPTIMIZATION

A single pixel APS circuit is proposed here which is designed by CNTFET. In this proposed design one extra transistor has been introduced to make the readout time faster. The circuit diagram is shown in Fig. 7.

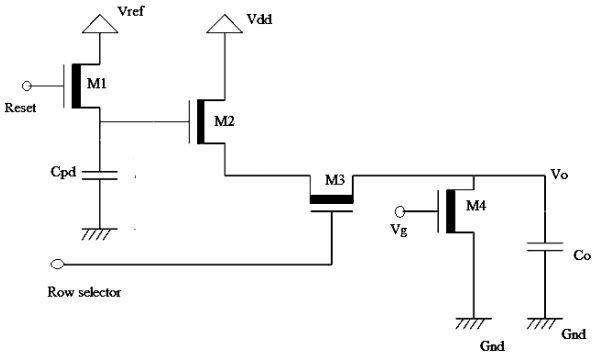

Figure 7. Proposed 4T based CNTFET APS cell

In the proposed design C_{pd} has been considered as the equivalent measurement of photodiode. M2 is the readout transistor. When reset of M_1 is high then V_{cpd} tends to be equal to V_{ref}. To maintain the readout, transistor M2 is kept always above the threshold voltage, V_{th}. We considered the following equation:

$$V_{ref} < V_{dd} - V_{th} \quad (13)$$

Because considering $V_{ref} = V_{dd}$ would make higher PDP. When $V_{cpd} = V_{ref}$ then the photo-current is integrated for a fixed period and it produces a voltage which is directly proportional to the incident light intensity. The integrated voltage V_{cpd} is converted to an output column current by transistor M_2 (Readout Transistor). So, this is like a trans-conductance amplifier. Assuming $V_a = V_o$ means no voltage drop in M_3 (Pass Transistor). Transistor M_4 has been introduced to reduce the readout time. The discharging time of the output capacitor, C_o could be made faster by using higher bias current (if only M2 operates in channel length modulation and $V_{ref} = V_{dd}$) but this will lead to higher power consumption. Therefore, V_{th} of M4 is kept lower and M4 is OFF when row selector is high and vice versa. To achieve this operation a column sensor circuit was coded in HSPICE so that M4 turns on when V_o is high, at the same time the row selector automatically becomes low.

A. Transient response of CNTFET APS circuit

Fig. 8, shows the transient analysis for the proposed CNTFET APS circuit for specific reset and row selector signal as well as V_g. At $10ns \leq t < 20ns$, when $V_{cpd} = 1$ then row selector = 1, $V_g = 0$ and V_o tends to be 1 (C_o is being charged). The intermediate signaling operations of row selector and V_g are done by a column sensor circuit which makes very fast readout operation when V_o reaches to 1. As in Fig. 8, at $t = 20ns$, when $V_o = 1$ then the column sensor circuit automatically triggers V_g as 1. Hence M4 is ON and it discharges V_o very fast due to optimized D_{CNT} of M4, at this time row selector is kept low.

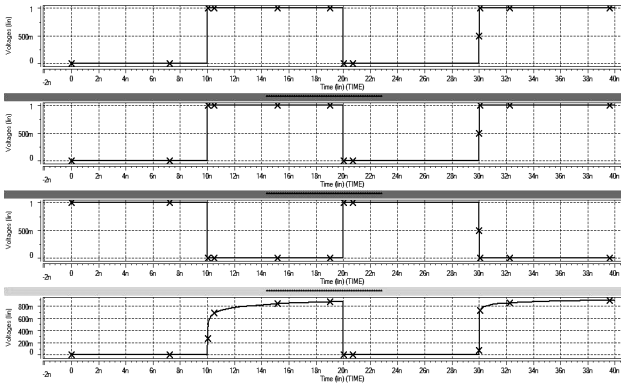

Figure 8. Transient analysis of the proposed 4T CNTFET APS cell

B. Chiral index optimization of the proposed CNTFET APS

Transient simulation is done for different values for chiral vector index, m. Here, Table II shows different values of D_{CNT} and V_{th} with respect to the change in chiral vector. The values of D_{CNT} and V_{th} have been calculated by using equation (3) and (4).

TABLE II.
CHIRAL INDEX, DIAMETER OF CNTFET (D_{CNT}), AND THRESHOLD VOLTAGE (V_{th})

Chiral Index, m	D_{CNT} (nm)	V_{th} (V)
6	0.469731	0.928244
7	0.54802	0.795638
8	0.626308	0.696183
9	0.704597	0.618829
10	0.782885	0.556946
11	0.861174	0.506315
12	0.939462	0.464122
13	1.01775	0.42842
14	1.09604	0.397819
15	1.17433	0.371298
16	1.25262	0.348092
17	1.3309	0.327616
18	1.40919	0.309415
19	1.48748	0.29313
20	1.56577	0.278473
21	1.64406	0.265213
22	1.72235	0.253157
23	1.80064	0.242151
24	1.87892	0.232061
25	1.95721	0.222779
26	2.0355	0.21421
27	2.11379	0.206276
28	2.19208	0.198909
29	2.27037	0.19205
30	2.34866	0.185649

Likewise the above tabulated data, here the power consumption, delay, and PDP are calculated from HSPICE simulation of the proposed CNTFET APS cell which has been shown in Table III.

TABLE III.
CHIRAL INDEX, POWER CONSUMPTION, DELAY AND POWER DELAY PRODUCT (PDP)

Chiral Index, m	Power Consumption (nw)	Delay (s)	PDP (ws)
6	3.84	1.23E-29	4.72E-38
7	7.96	1.23E-29	9.79E-38
8	11.0	1.23E-29	1.35E-37
9	13.4	1.23E-29	1.64E-37
10	15.3	1.23E-29	1.88E-37
11	16.8	1.23E-29	2.06E-37
12	28.6	1.23E-29	2.20E-37
13	32.7	7.89E-20	1.48E-27
14	36.8	7.08E-20	1.37E-27
15	40.9	6.55E-20	1.30E-27
16	45.0	6.24E-20	1.27E-27
17	49.2	6.06E-20	1.21E-27
18	21.2	5.84E-20	1.23E-27
19	21.7	5.68E-20	1.23E-27
20	22.2	5.70E-20	1.26E-27
21	22.3	5.72E-20	1.27E-27
22	22.6	5.78E-20	1.30E-27
23	23.1	5.93E-20	1.37E-27
24	23.8	6.69E-20	1.59E-27
25	24.0	6.92E-20	1.66E-27
26	24.6	7.27E-20	1.79E-27
27	25.2	7.57E-20	1.90E-27
28	25.5	7.87E-20	2.01E-27
29	26.1	8.18E-20	2.13E-27
30	26.6	8.49E-20	2.26E-27

From Table III, a 3D graph is plotted in OriginPro shown in Fig. 9 and the optimum chiral, m is found to be 19. For this value of m, the threshold voltage is minimal which is only 0.2931V and other parameters are relatively optimal. So V_{ref} is also set from equation (13) as follows:

$$V_{ref} < 1 - 0.2931$$
$$=> V_{ref} < 0.7069$$

Now, if V_{ref} is kept lower than V_{th} then APS circuit cannot operate. So the reference voltage, V_{ref} is set to 0.70V in the proposed design so that the power consumption is low and also the circuit can operate effectively.

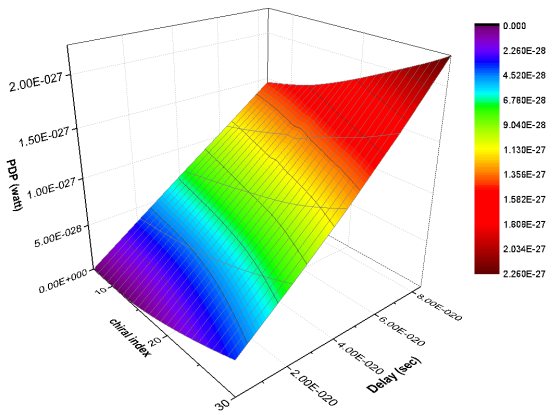

Figure 9. PDP vs. chiral index, m vs. delay

VII. PERFORMANCE ANALYSIS OF THE PROPOSED DESIGN

The APS circuit performance can be determined by its frame rate and quality of the pixel. The frame rate is higher when the readout time is significantly lower. From the optimized simulated results worked out by HSPICE, the readout time of the proposed CNTFET APS cell (22nm process) is found 8.2495ps whereas from a related paper [1], the 4T based CMOS APS cell (0.35µm process) has approximately 4.1µs readout time. Also it has been found that by considering the same proposed design based on CMOS and CNTFET with same process length (22nm), the CNTFET APS performs the way faster and yields better results in terms of power consumption and delay. Also Section VI proves the better performance of CNTFET logic over CMOS logic.

A. Biasisng effect and readout time

Biasing currents and readout times are observed by varying the gate voltage of M4 in the proposed design. From HSPICE analysis, the optimal bias current is found to be approximately 0.014nA and for this value of bias current the corresponding value of V_g = 0.37V is selected for the optimization of proposed design. Moreover, the achieved HSPICE data in Table IV show that even though bias current is increased above 0.014nA, the change of readout time as well as PDP are not that significant while V_g has to be increased up to V_{dd} which would eventually increase the overall PDP of the APS cell. Readout time vs. bias current is shown in Fig. 10.

TABLE IV.
BIAS CURRENT, DELAY, AND PDP TABLE

Gate voltage,V_g	Bias Current (nA)	Readout Time (ps)	PDP (ws)
0.30	0.010700	15.735	5.0935E-19
0.35	0.010534	13.366	2.6477E-19
0.40	0.019084	9.4364	1.8567E-19
0.50	0.062410	9.3441	1.8439E-19
0.60	0.063035	8.9251	1.6610E-19
0.65	0.065721	8.7472	1.7523E-19
0.70	0.14711	8.5525	1.8033E-19
0.75	0.20196	8.4568	1.6865E-19
0.85	0.28961	8.3650	1.7377E-19
0.90	0.33709	7.6621	1.6060E-19
0.95	0.38593	7.6679	1.6195E-19

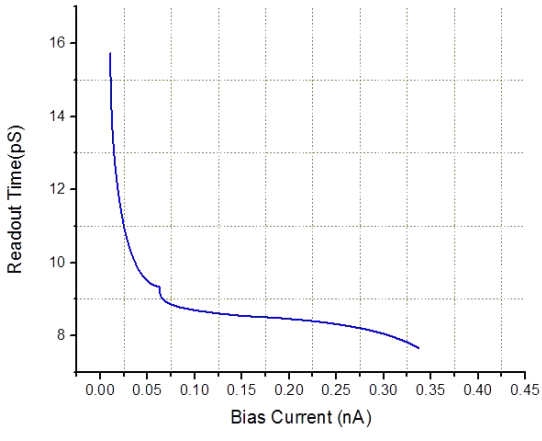

Figure 10. Readout time vs. bias current

In Fig. 10 it is observed that the readout time decreases when bias current increases. PDP vs. bias current is shown in Fig. 11. The change of readout time and PDP is not linear with the change of bias current of M4.

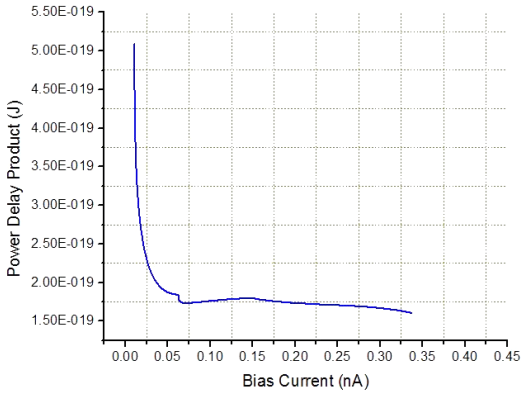

Figure 11. Power delay product vs. bias current

B. *Effect of varying load capacitance over readout time*

Fig. 12 shows the readout time vs. the variation of the load capacitor.

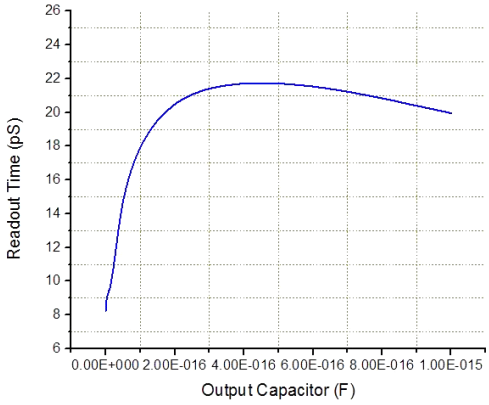

Figure 12. Readout time vs. load capacitor

To find the suitable load capacitor the rest parameters in the proposed design are set to the optimum value during the simulation. The optimum value of C_o is picked when the output voltage is saturated. A value of 1e-9fF load capacitor can perform the preeminent result in CNTFET APS cell.

VIII. CONCLUSION

In this paper a single pixel 4T based CNTFET APS is designed. The performance of the proposed design has been also compared to CMOS APS circuit in terms of readout time. Since the achieved readout time in CNTFET APS is immensely reduced than that of CMOS APS, hence obviously higher frame rate can be achieved from the proposed design. For improving the frame rate primarily the readout time was reduced by introducing one extra transistor to the output capacitor as well as the column sensor circuit. This transistor was also uniquely biased for faster discharging operation and thus resulted a significant amount of time decrease. Optimized capacitor value was taken for better output and faster discharging time as well. Overall, the proposed design is proven to be a high frame rate capable CNTFET APS cell for Nanoelectronics as well as Ultra Low Power Devices (ULPDs).

REFERENCES

[1] K. Salama, and A. El Gamal, "Analysis of Active Pixel Sensor Readout Circuit," *IEEE Transactions on Circuit and Systems-1: Fundamental Theory and Application*, Vol. 1, No. 7, July 2003. http://dx.doi.org/10.1109/TCSI.2003.813977

[2] S. J. Tans, A. R. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature,* Vol. 393, Issue 6680, pp. 49-52, May 1998. http://dx.doi.org/10.1038/29954

[3] S. Iijima, "Helical microtubules of graphitic carbon," *Nature* 354.6348 (1991): 56-58. http://dx.doi.org/10.1038/354056a0

[4] P. L. McEuen, M. Fuhrer, and H. Park, "Single-Walled Carbon Nanotube Electronics," *IEEE Transactions on Nanotechnology*, Vol. 1, No. 1, March 2002. http://dx.doi.org/10.1109/TNANO.2002.1005429

[5] N. Wang, Z.K. Tang, G.D. Li, and J.S. Chen, "Single Walled 4Å carbon nanotube arrays," *Nature*, Vol. 408, pp 50-51, Nov 2000. http://dx.doi.org/10.1038/35040702

[6] J. Deng, and H. -S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region," *IEEE Trnsactions on Electron Devices*, Vol. 54, No. 12, pp. 3186-3194, December 2007. http://dx.doi.org/10.1109/TED.2007.909030

[7] (2008) Stanford University CNFET Model, Stanford University, Stanford, CA. [Online]. Available: https://nano.stanford.edu/stanford-cnfet-model

[8] (2008) Predictive Technology Model (PTM), Arizona State University, Tempe, AZ. [Online]. Available: http://ptm.asu.edu

[9] M. H. B. Jamaa, K. Mohanram, and G. D. Micheli, "Power consumption of logic circuits in ambipolar carbon nanotube technology," *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2010 , pp.303-306, 8-12 Mar. 2010. http://dx.doi.org/10.1109/DATE.2010.5457189

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