Rapid Development of System-on-Chip (SoC) for Network-Enabled Visible Light Communications

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Abstract—Visible Light Communication (VLC) is an emerging optical communication technology with rapid development nowadays. VLC is considered as a compliment and successor of radio-frequency (RF) wireless communication. There are various typical implementations of VLC in which one of them is for exchanging data TCP/IP packets, thus the user can browse the internet as in established Wireless fidelity (Wi-Fi) technology. Briefly, we can call it by Light fidelity (Li-Fi). This paper described the design and implementation of System-on-Chip (SoC) subsystem for Li-Fi application where the implemented SoC consists of hardware (H/W) and software (S/W). In the H/W aspect, Physical Layer (PHY) is made by using UART communication with Ethernet connection to communicate with Host/Device personal-computer (PC). In the S/W aspect, Xillinux operating system (OS) is used. The H/W- as well as S/W-SoC, are realized in FPGA Zybo Zynq-7000 EPP development board. The functional test result shows (without optical channel or Zybo-to-Zybo only) that the implemented SoC is working as expected. It is able to exchange TCP/IP packets between two PCs. Moreover, Ethernet connection has bandwidth up to 83.6 Mbps and PHY layer *baud rate* has bandwidth up to 921600 bps.

Keywords—Light fidelity (Li-Fi), Physical layer, System-on-Chip, Visible Light Communication, Xillinux OS

1 Introduction

Mobile data traffic which grows exponentially for the last two decades has caused extreme wireless network usage. As the impacts, the available RF spectrum will be greatly reduced. Then the channel interference will be higher **[1]**. The year 2021 worldwide estimated there are more than 49 exabytes (Note, 1 EB = 1 billion gigabytes) of data traffic from the mobile-network in every month **[2]**. One solution is to replace the common RF-based technologies (like Wi-Fi) with another technology which employs beyond the RF spectrum. Visible light (380 nm – 780 nm) is considered spectrum to be employed for high-speed internet access purpose with no elec-

tromagnetic interference, highly secure communication, no licensed bandwidth, and no health concern **[3]**, this technology commonly called as Li-Fi **[4]**.

Li-Fi system is built by two blocks: the digital part and the analog part. Similar with Wi-Fi, the Li-Fi must offer an extremely high-speed internet connection to the user. Therefore, a very fast microprocessor system is needed for Li-Fi application in order to process the fastest data. The field-programmable gate array (FPGA) is more feasible to utilize compared to general microcontroller for high-speed DSP application **[5]**. That is why this work uses SoC platform as a digital processor in VLC system. The SoC is an integrated circuit containing all components of an electronic system or computer on a single-chip. With SoC technology, the bulky VLC system (because of using commercial off-the-shelf devices) as reported so far, will be minimized drastically in terms of size **[6]**. SoC VLC is an emerging technology.

In previous research, we have implemented SoC VLC but it is functionalized for high-speed data acquisition only in receiver system **[7]**. In this paper, the designed SoC architecture focuses to process the 'TCP/IP packet' for Li-Fi applications. The Specifications for SoC are able to: 1) exchange data between two computers; 2) convert data packet to bit-level transmission; and transmit the data with maximum *baud rate* (921600 bps) by UART communication. The defined specifications will be the reference in design and implementation phase (Section II). Whereas the discussion performance tests are presented in Section III.

2 Methodology

2.1 Network Topology and Data Exchange Mechanism

Based on the defined system specifications, there are two units of the personal computer node to be used, for Host and then Device function. Commonly, network topology for two nodes employs point-to-point (P2P) topology **[8]**. In order for this two nodes that able to exchange data through the links, it is necessary to set the appropriate IP address, DNS Server, MAC address, and Gateway address. The selection of IP Address and MAC Address are arbitrary, while DNS is set with 8.8.8.8 (Google's public DNS). The connection design for two nodes is depicted in Fig. 1.

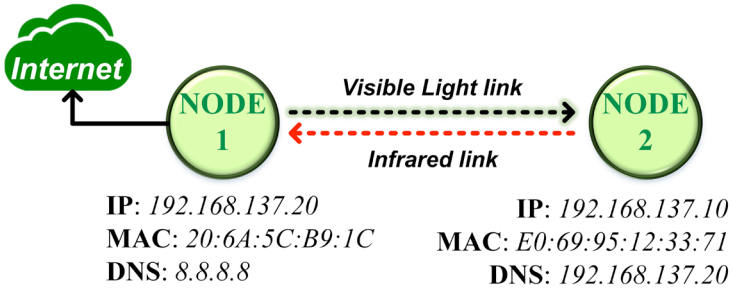


Fig. 1. Node and address setting diagram

The data exchanges (TCP/IP packet) between two nodes can be classified into two sides, *i.e.* device to host and device to device. In this work, the PHY layer development is not focused on IEEE 802.15.7 standard compliance. Therefore, we used Reed-Solomon (RS) and UART.

At the personal computer to FPGA Zybo part, the data exchange is done by using Ethernet connection via LAN cable where it is chosen because of the common wired internet connectivity. Furthermore, FPGA Zybo is equipped with complete peripherals that also supports Ethernet connexion. The connection diagram is shown in Fig. 2(a). While for Zybo to Zybo part, the data exchange is done by using UART communication as illustrated in Fig. 2(b). The complete diagram is shown in Fig. 3.

As described previously, the P2P topology for this work is used two FPGA Zybo boards and two personal computers. The following a step by step for the IP Address and DNS setting in Windows 2010 OS: Start ➔ Settings ➔ Network and Internet ➔ Ethernet ➔ Change adapter options ➔ Double-click Ethernet ➔ Double-click Internet Protocol version 4 (TCP/IP v4) until the properties appears as visualized in Fig. 4(a), while for Linux OS (in FPGA Zybo), IP Address and DNS setting is by right-clicked on network icon (in the upper right corner) then 'Edit Connections' as visualized in Fig. 4(b).

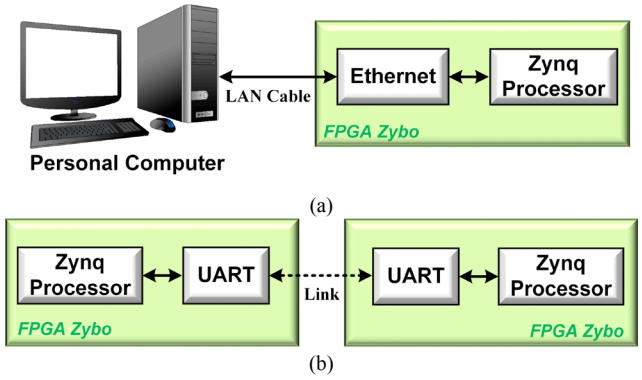


Fig. 2. The diagram of data exchanges: (a) device to host; (b) device to device

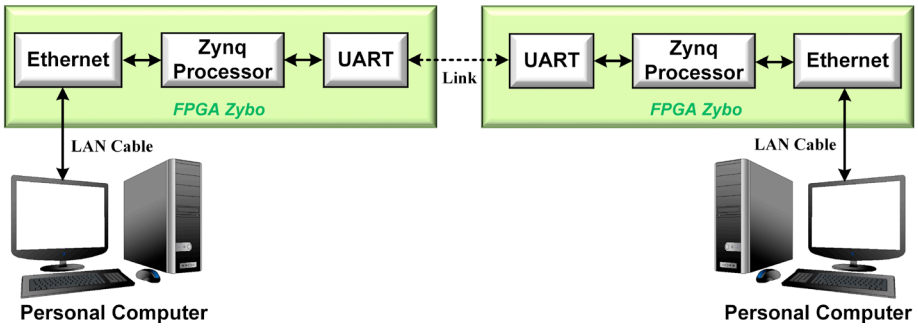
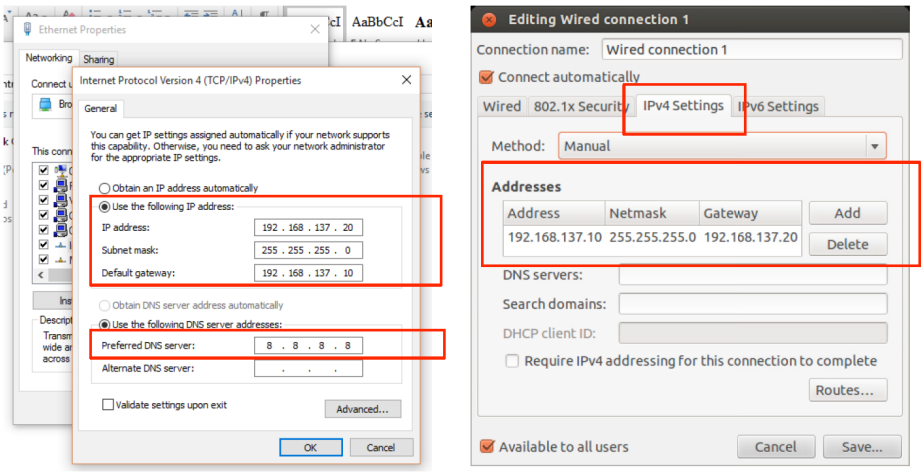


Fig. 3. Complete diagram of data exchange mechanism



(a) (b)

Fig. 4. Screenshot of configuration setting for: (a) IP address and DNS address in Windows 10 OS; (b) IP address and Gateway in Linux OS

Ethernet connection has been already activated, so there is no need to configure it manually in FPGA Zybo. Fig. 5 shows the *ifconfig* command in FPGA Zybo, it can be shown that *eth0* (first Ethernet interface) has been configured.

For the universal asynchronous receiver-transmitter (UART) communication, the peripheral is generated by using Vivado 2015.1 software. Moreover, the DTB file is also need to be modified so Xillinux OS can recognize the added UART peripherals. Fig. 6 visualizes the UART enabling process, whereas Fig. 7 visualizes the UART peripheral that has been created.

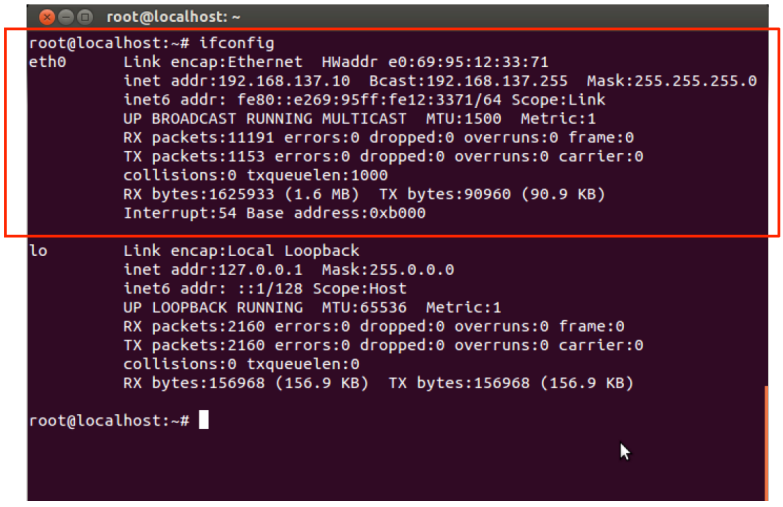


Fig. 5. Performance test for device to host scheme

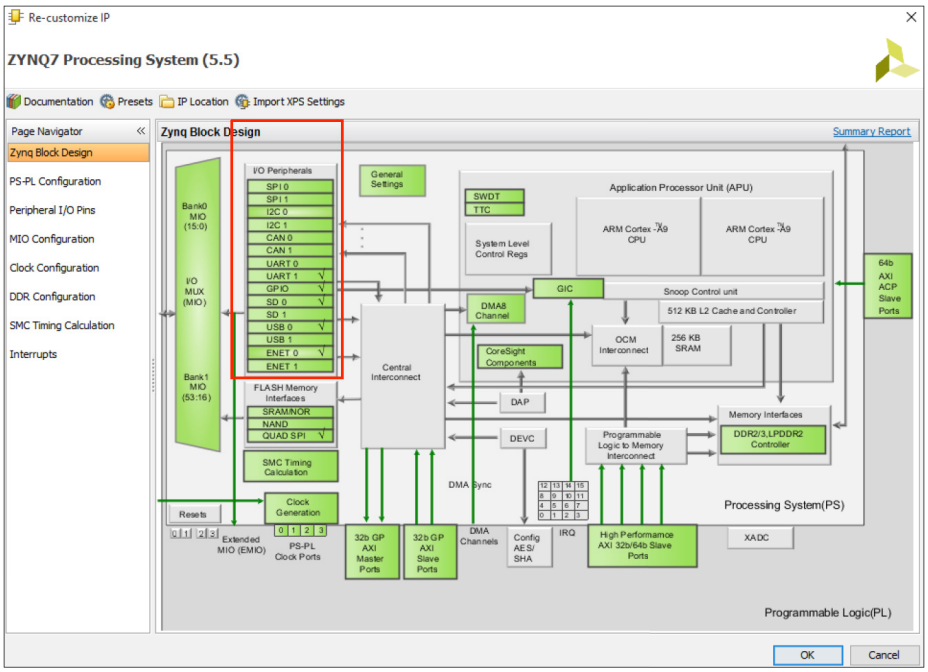


Fig. 6. The peripherals activation on Vivado 2015.1, the DTB must be generated from the DTS source code (Please see its code in the supplementary file of this paper)

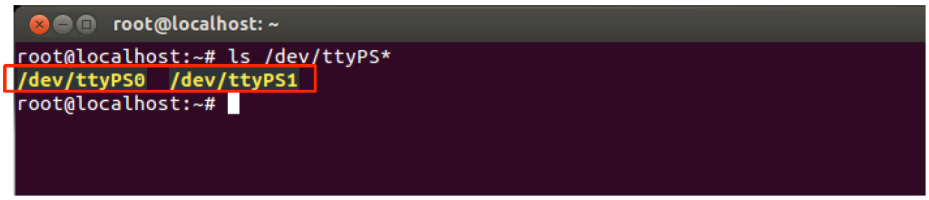


Fig. 7. UART peripheral (*ttyPS0*), we can see that *.ttyPS1* already exists by default

2.2 Xillinux OS

In previous work, we have developed MAC Layer software that is written in Python script **[9]**, to execute this programs, we need an OS. The FPGA Zybo board has ARM-based processor that capable to run the Linux OS. There are several Linux OS distributions can be run by FPGA Zybo, one of them is Xillinux OS that is chosen in this work because of it can communicate directly with FPGA fabrics and also able to access Ethernet and UART peripherals **[10]**. To perform the booting process, FPGA Zybo needs to perform several boot stages as depicted in Fig. 8.

The FPGA Zybo employed SD Card media storage to boot Xillinux OS. Therefore, it should be formed into 2 partitions: ***FAT32*** and ***EXT4*** file system. The ***FAT32*** partition comprises *u-boot.bin* (merged into a *boot.bin file*), *FSBL file*, Linux Kernel

(named as *uImage*), and *Bitstream PL* (written as *xillydemo.bit*). While **EXT4** partition comprises Linux RAM Disk. Those files are generated by using Vivado 2015.1 software and placed in the **FAT32** partition. Generated files should look like visualized in Fig. 9. If the structure of these required files is correct, the SD Card can be booted well and vice versa.

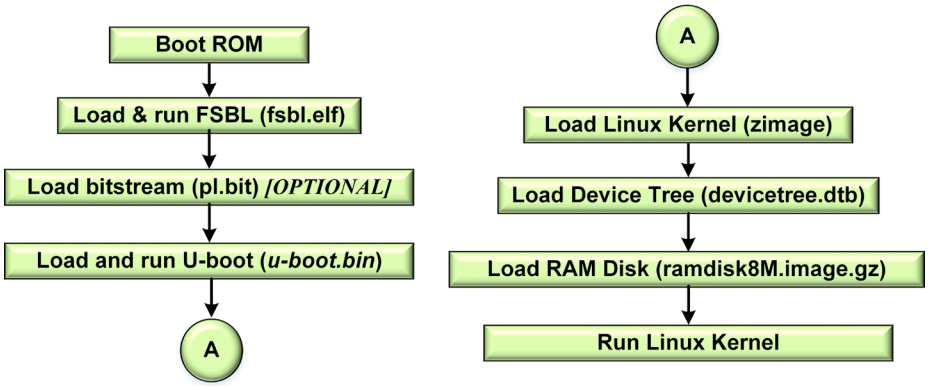


Fig. 8. Flowchart of Linux booting in FPGA Zybo, reproduced from **[11]**

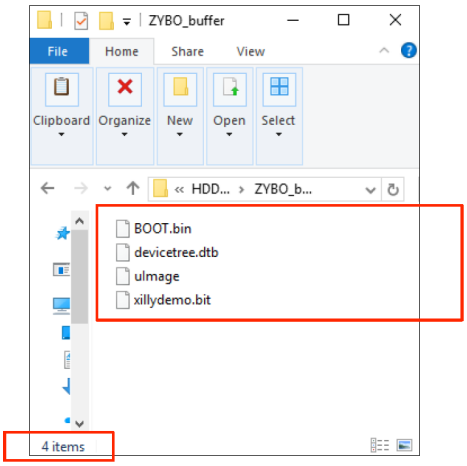


Fig. 9. File structure of Xillinux OS

2.3 Forward Error Correction (FEC)

The FEC is a method to recover error from data transmission by sending redundant data. As stated by IEEE 802.15.7 standard, the FEC for PHY layer of VLC is RS code or *RS*(*n,k*) method **[12]**. In brief, the principle of work: the data entered through the RS encoder will occur the addition of bits to overcome the error. Later, the received data will also be recovered and re-read by the RS. We used *RS(64,32)* means 64-bit of block length, 32-bit of input data length, and 16-bit of parity.

In this work, FEC RS is created by using freely available online library that is written in Python script (please see the FEC RS open source code in the following link: https://github.com/jkent/minimodem-crypt/blob/master/minimodem-crypt/reedsolo.py).

2.4 Overall Design of SoC

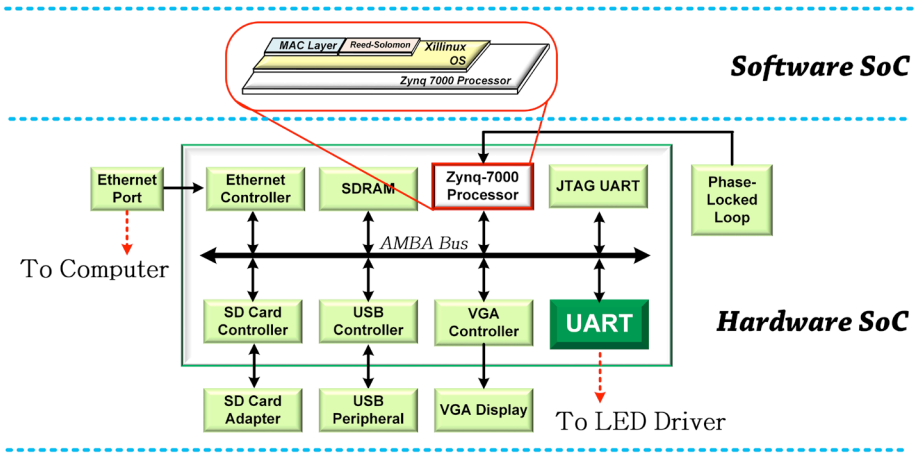


Fig. 10. Architecture of the designed SoC for network-enabled VLC

Table 1. The use of register address mapping

Register Base Address	Description
E000_0000, E000_1000	UART Controllers 0, 1
E000_2000	USB Controllers 0
E000_B000	Ethernet Controller 0
F800_6000	SDRAM
E010_0000	SD Card Controller
5000_1000	VGA Controller

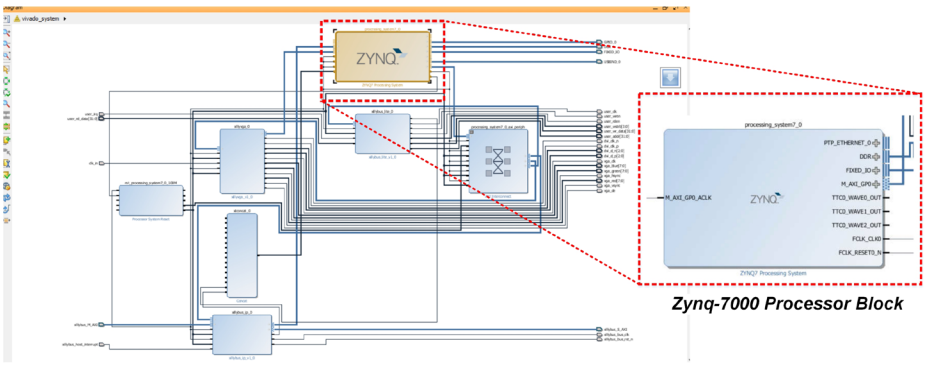


Fig. 11. Implementation of Zync-7000 processor blocks on FPGA Zybo

The designed SoC as illustrated in Fig. 10 consists of two parts: Software (S/W) and Hardware (H/W). The S/W part comprised operating system, Reed-Solomon software, and MAC Layer software while H/W part comprised the components used, register settings which used to access the H/W as shown in Table 1 and design architecture. The implementation of processor block is done by using Vivado 2015.1 software, this block will run Xillinux OS, process the MAC layer part, and execute the RS code.

3 Results

3.1 Functionality test of Xillinux OS

The functionality test of Xillinux OS ensures that it is ready to be employed in developing the required software include booting up as visualized in our previous research **[13]**, loading the standard user interface as depicted in **[9]**, and running the Python script as shown in Fig. 12.

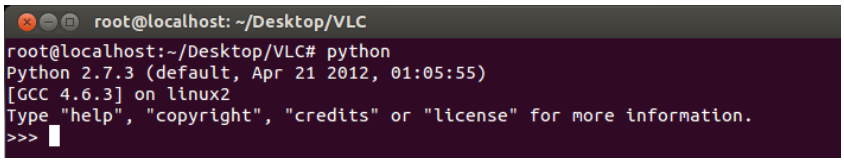


Fig. 12. The Python programs can be run through the Terminal

3.2 Bandwidth of Ethernet and UART

In this work, we performed two measurements: bandwidth of Ethernet and UART. The Ethernet bandwidth measurement is done by using *iperf* tool as shown in Fig. 13. We obtained 83.6 Mbps of average bandwidth.

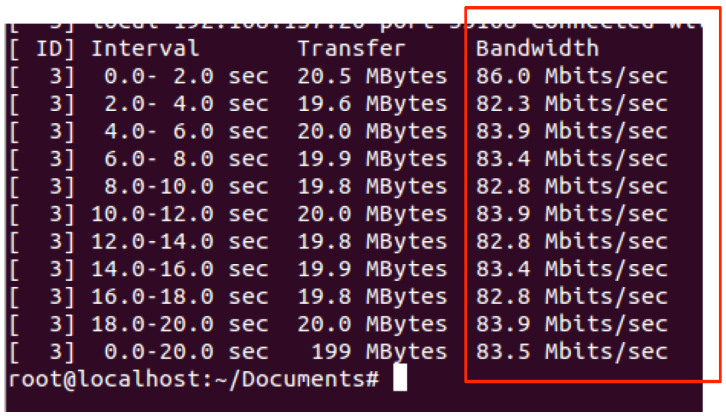


Fig. 13. Measurement of Ethernet bandwidth with *iperf* tool

While UART bandwidth measurement is done by using Python script which is sending serial data in certain *baud rate*. We obtained 921600 bps of maximum *baud rate* and it can be lowered down to 115200 considering to the capability of the LED driver input frequency.

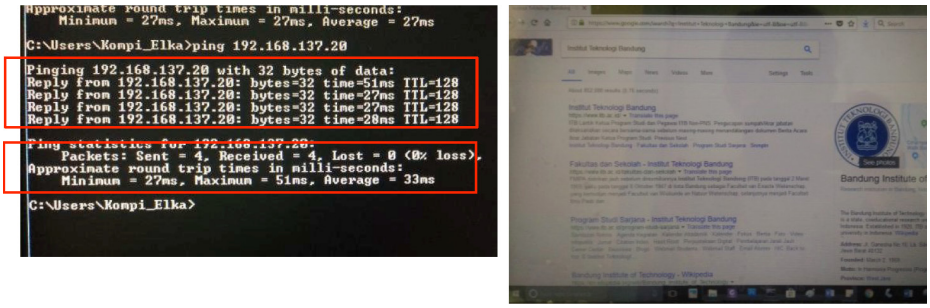
Bandwidth measurement of UART

```
root@localhost:~/Desktop/VLC# python pure.py/dev/ttyPS1
Baudrate: 115200 bps
hello world! 0
hello world! 1
hello world! 2
hello world! 3
hello world! 4
hello world! 5
hello world! 6
hello world! 7
hello world! 8
hello world! 9
hello world! 10
root@localhost:~/Desktop/VLC# python pure.py/dev/ttyPS1
Baudrate: 921600 bps
hello world! 0
hello world! 1
hello world! 2
hello world! 3
hello world! 4
hello world! 5
hello world! 6
hello world! 7
hello world! 8
hello world! 9
hello world! 10
hello world! 11
root@localhost:~/Desktop/VLC#
```

3.3 Overall Test

We have performed functional test of RS, the input of RS is TCP/IP packet data where its input is always an integer. The decoding result of RS is then compared with the input to find the error value. The result of performance test shows that the implemented RS can detect error occurs in the communication system.

The evaluation of overall system is by doing ping and browsing the internet. Fig. 14(a) visualizes the ping testing result, we obtained 33 milliseconds of average latency. Fig. 14(b) proves that internet browsing successfully demonstrated (in this term, we used Google search engine). Therefore, FPGA-based VLC (Li-Fi) is able to exchange network packet (TCP/IP). Thus, it allows users to "surfing" and "browsing" to the internet such as Wi-Fi technology. It should be noted that in this evaluation, we test our SoC by following scenario: FPGA Zybo transmitter to FPGA Zybo receiver. It means that analog front-end module is not connected yet.



(a) (b)

Fig. 14. Screenshot of: (a) Ping test result between two computers (Host-to-device); (b) successful internet browsing in searching the keywords of "Institut Teknologi Bandung"

4 Conclusions

We can conclude several key points for this work, i.e. 1) SoC subsystem has been designed and carefully implemented, and also already demonstrated successfully to perform Ping and browsing the internet; 2) the average of Ethernet bandwidth is 83.6 Mbps; 3) the maximum bandwidth of UART communication is 921600 bps. For future work, we will integrate our DSP (FPGA Zybo) with analog front-end part.

This work has strong correlation with the works. To track our research results and to know the relationship among others, the readers can find the following reference **[14-35]**. Later, the PHY layer on our Li-Fi subsystem can also be improved by designing RS based on H/W, then adding *RLL 8B10B* and Manchester Encoding.

5 Acknowledgment

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