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PAPER

Enhancing Power Electronics Labs through Error-Based and Self-Regulated Learning

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ABSTRACT

This paper presents a technology-enhanced pedagogy for power-electronics labs. It combines self-regulated learning (SRL) and error-based learning (EBL). The approach guides students through three phases: forethought, performance, and reflection. Each phase uses formative checks, scaffolded feedback, and opportunities to retry. We implemented two modules: AC–AC and DC–AC converters. Both are run on microcontroller-based boards with real instruments. Oscilloscopes and Fast Fourier Transform (FFT) and Total Harmonic Distortion (THD) analyze errors in real time. We collected three Likert-scale surveys: one on the method and two on the lab modules. The students reported high satisfaction (≈4.5/5). They would recommend this method and felt more confident in facing mistakes. The results also show the role of difficulty and logistics in the task. These factors suggest more scaffolding for complex work. We conclude with design principles for SRL-oriented EBL in engineering laboratories. The principles focus on clear feedback loops, visible error signatures, and deliberate practice. The study offers practical guidance for postsecondary technology-enhanced learning.

KEYWORDS

self-regulated learning (SRL), error-based learning (EBL), technology-enhanced learning, power electronics, microcontroller-based labs, fast fourier transform (FFT) or total harmonic distortion (THD), formative assessment

1 MOTIVATION

Power-electronics education needs a bridge between concepts and practice. Students often struggle when theory meets noisy, real signals. Technology can reduce this gap. It can make errors visible and actionable in the lab. Self-regulated learning (SRL) offers a cycle for that work. Error-based learning (EBL) turns mistakes into feedback and growth. Together, SRL or EBL form a simple loop. Plan, act, reflect, and try again. Microcontroller-based rigs and standard instruments support this loop. Oscilloscopes and Fast Fourier Transform (FFT) or total harmonic distortion (THD)

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analysis expose error signatures in real time. Short feedback cycles promote agency and confidence. This results in a deeper understanding and better troubleshooting. This paper presents a practical, technology-enhanced design for that goal in a post-secondary course.

2 CONTRIBUTION STRUCTURING

This paper reports on a complete, technology-enhanced intervention for a power-electronics lab. The contribution has four parts.

1. Pedagogical framework. We define the SRL or EBL cycle in a laboratory context. We explain how technology enables short, formative feedback loops.
2. Materials and methods. We describe two modules (AC–AC and DC–AC). We specify hardware, measurement setup, and procedures. We detail instruments, signals, and data capture for FFT or total harmonic distortion.
3. Results. We present student perceptions and usage evidence. We report key patterns that emerge during error diagnosis and re-attempts.
4. Discussion and conclusion. We interpret the findings against previous work. We distill design principles for SRL-oriented EBL with real instruments. We outline limits and future extensions.

3 INTRODUCTION

Engineering education faces growing technological complexity and diverse competence demands. Programs must connect theory with practice in authentic settings. Technology-enhanced learning (TEL) supports this goal. Structure SRL cycles and short feedback loops that make progress visible and timely [1]. Structured state-of-the-art analyses help the community judge relevance without reading the entire literature; they show how to synthesize previous work and identify gaps that matter to the field [2], [3]. Some reviews also outline research agendas for technology-enhanced designs in higher education and stress iterative development under authentic constraints [4].

Within this framework, EBL treats mistakes as data for improvement rather than failure. The formal assessment clarifies the gaps and guides corrective action [5]. Feedback can have strong effects on achievement when it specifies goals, progress, and next steps [6]. The classic work also defines conditions for the effective formative use of criteria, comparison, and correction [7]. Sustainable feedback extends these effects over time and builds student agency [10]. From a constructivist stance, knowledge develops through activity, interaction, and the resolution of cognitive imbalance [8], [9].

The literature reveals clear trade-offs between delivery modes and scaffolding. Online or simulation-only studies scale well and reduce authenticity. Hands-on labs provide rich signals and tacit skills and increase costs and logistics. Strong scaffolding lowers frustration for novices and may limit autonomy. Light scaffolding fosters agency and can increase error rates and variability. This study addresses these trade-offs in a power electronics course shared by electrical engineering and industrial electronics and automation. Students work with programmable microcontroller-based boards, adjust firing angle and pulse-width modulation (PWM) parameters, and observe immediate effects on the output signal. Oscilloscopes and FFT and THD analysis make error signatures visible and support rapid re-attempts. The design aligns the formative and sustainable feedback principles [5], [10] and builds on previous active-learning work in technical subjects, including flipped classroom and project-based learning (PBL) [11].

The paper examines how real-time instrumented feedback cycles operationalize SRL in higher engineering education in power-electronics laboratories, the extent to which an EBL design shapes how students perceive learning and error-handling efficacy, and the design principles that enable replicable TEL implementations in engineering laboratories.

4 METHODS

This section explains the setup so that an experienced instructor can repeat the study. Covers research design and context, the technology stack, replicable procedure, two laboratory lines, measures and instruments, and the analysis that links the method elements to outcomes. Figure 1 summarizes the SRL or EBL core cycle, and Figure 2 outlines the session flow. Appendices A to C provide replication materials.

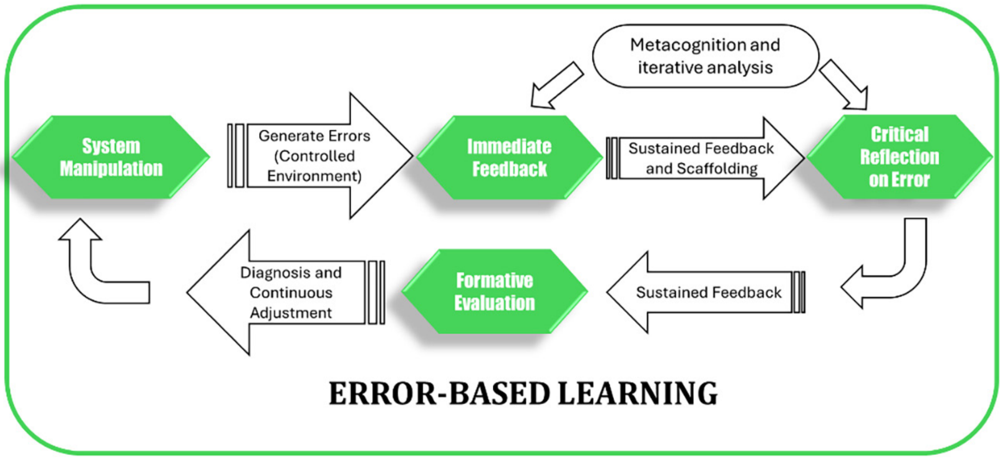

Fig. 1. SRL or EBL cycle in technology-enhanced power electronics labs[1]

Regarding research design and rationale, we use a mixed-methods design to capture cohort trends and explain patterns. The quantitative strand relies on Likert surveys. The qualitative strand uses open responses and lab artifacts. The study is aligned with design-based principles in higher education to iterate under authentic constraints [4]. The pedagogical frame combines EBL and SRL with short cycles of planning, action, reflection, and re-attempt. Goals of the formative and sustainable feedback structure, progress, and next steps [6], [10]. Classic conditions of criteria, comparison, and correction guide checkpoints [7].

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[1] Formative evaluation → system manipulation → immediate scaffolded feedback → critical reflection and re-attempt. Error signatures are visible in real time with oscilloscopes, FFT, and THD.

Concerning setting up and participants, the intervention is run in a power electronics course shared by electrical engineering and industrial electronics and automation programs. Both cohorts follow the same SRL or EBL core. The electrical engineering group emphasizes conversion in renewable systems. The industrial electronics group emphasizes converter design and control. All activities take place in scheduled classes and laboratories.

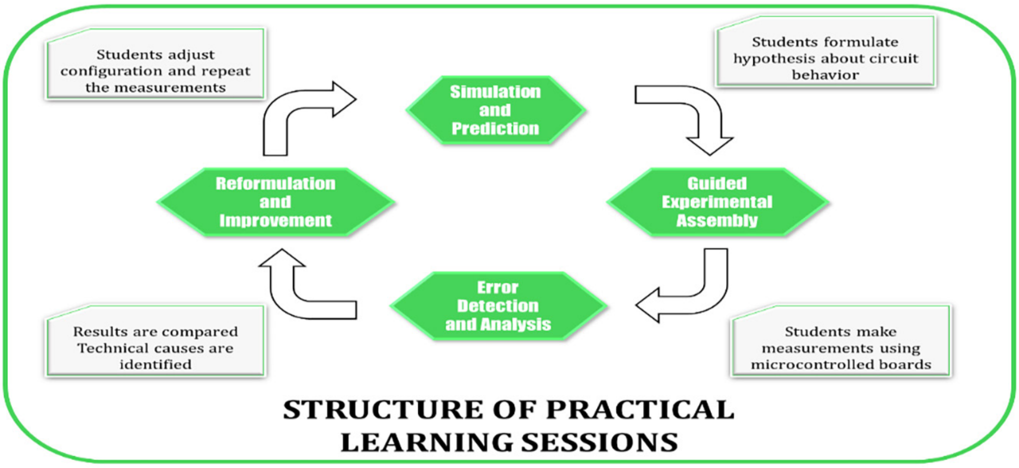

Fig. 2. Session flow[2]

With respect to materials and technology-enhanced learning infrastructure, students work with microcontroller-based boards configured by software. They adjust the firing angle, frequency, control mode, and pulse-width modulation (PWM) duty cycle. We used a digital oscilloscope and computer, FFT, and THD. This setup makes error signatures visible in real time and supports fast iteration. Evidence from virtual or remote laboratories motivates the focus on engagement and continuity, which we port to a face-to-face setting with repeatable tasks [12]. We also take cues from labs that have the Internet of Things (IoT) enabled to favor affordable hardware and remote-ready protocols when an extension is required [13].

Regarding the procedure, each activity uses a lab sheet (refer to Appendix A) with goals, risks, parameter ranges, and acceptance criteria. The sequence starts with a brief recap of the theory. Students predict with a simulation and then implement it on the board. They diagnose deviations between expected and observed signals. The instructor provides scaffolded feedback through guiding questions. Students re-attempt and document the improvement. The loop repeats until the rubric thresholds are met, as summarized in Figure 1 and operationalized at the session level in Figure 2.

In theory–practice coordination, laboratory work begins after two aligned theory sessions. Each lab opens with a recap of signals, constraints, and safety. Exams in theory reveal error patterns that often reappear in the lab. During the review, the instructor classifies errors as conceptual, computational, or formal and discusses the consequences of troubleshooting.

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[2] Simulation and prediction → guided assembly → error detection and analysis → reformulation and improvement. Side tasks: hypothesis setting, microcontroller measurements, comparison and cause identification, and repetition-level parameter readjustment.

For differentiated laboratory tasks, the same sequence applies to two converter lines, according to each degree profile. In Electrical Engineering, students use an AC–AC board and explore five modes: total phase control, total cycle control, differential phase control, differential cycle control, and cycloconverter. Oscilloscope traces and FFT reveal spectral artifacts due to commutation choices. In Industrial Electronics and Automation, students use a DC–AC inverter and tune the PWM frequency and duty cycle, evaluate the behavior in time and frequency, and compute THD. Group analysis links unstable or inefficient regimes to parameter windows. A common rubric evaluates documentation, signal analysis, and argumentation.

In measures and instruments, we deploy three surveys: one global for methodology and two module-specific for AC–AC and DC–AC. The items target perceived learning, error-handling efficacy, clarity and timeliness of feedback, and workload. SRL-related items cover planning, monitoring, and help-seeking using validated approaches in TEL [14]. The validity of the content is checked by expert review. Internal consistency is assessed with Cronbach's alpha at the scale level. We also collect artifacts such as configuration logs, waveforms, FFT or THD snapshots, and lab notes.

Regarding data analysis and method–result traceability, we compute descriptive statistics and check distributions. When assumptions do not hold, we use non-parametric tests and report effect sizes. Each survey construct maps to the method step that could influence it. For example, clarity of feedback links to the feedback step, and confidence in handling errors links to diagnosis and re-attempt. We code open responses thematically. Two coders label segments and resolve disagreements through discussion. Codes trace to artifacts to confirm or refine interpretations. Appendix B links each result variable to the method element that could generate it, allowing readers to judge the methodological suitability.

Concerning the adaptation and impact of the method, mixed methods counteract the limitations of single-strand designs. Surveys cover a wide range. Artifacts and comments explain the mechanisms. Design-based principles adapt to the time and equipment constraints in higher education [4]. Each adaptation appears on the lab sheet with its expected impact on validity. For example, capped lab time may reduce reattempts. We record the remaining gaps and plan follow-ups.

For emotional climate and safety, we frame error as informative to reduce anxiety and support resilience in converters with narrow margins and high cognitive load. Safety checklists prevent unsafe configurations. The instruments are calibrated before each session. The norm is safe, explainable, and repeatable.

Finally, the replicability package includes three elements. Appendix A contains the lab sheet template. Appendix B provides the method-to-result traceability table. Appendix C describes the bill of materials with acceptable ranges. These materials allow for replication and local adaptation.

With respect to the measurement model, sampling, and reliability, we report the approach to transparency. Two parallel cohorts participated. The electrical engineering group emphasized AC–AC, and the industrial electronics and automation group emphasized DC–AC. All activities occurred in scheduled classes and laboratories. Survey participation was voluntary and anonymous. Response rates were recorded at the cohort level. Survey items aligned with the constructs used in the results. These constructs were perceived learning, error-handling effectiveness, clarity and timeliness of feedback, workload, and module-level indicators such as guide clarity, usefulness of the setup, and value versus simulation. All items used a 1 to 5 Likert scale. Two instructors reviewed the clarity and alignment of the items. A short pilot confirmed unambiguous wording and the match with the step-wise lab sequence in Appendix A. Reliability was assessed at the construct level with Cronbach's alpha and 95% confidence intervals. Ordinal alpha was considered when assumptions were not met. The reliability coefficients and the item-to-construct map are summarized in Section 3.2; the full instrument and aggregate data are available upon request.

5 RESULTS

This section reports findings without interpretation. All items use a 1 to 5 Likert scale (5 = highest). Tables 1–3 summarize the cohort and item-level descriptive, and Figures 3 to 5 provide visual summaries. For the overall methodology (EBL), the mean rating was **4.50/5**. Students reported that they would recommend the method (**4.86**). They also noted greater confidence when facing new assessments (**4.57**) and perceived grade improvement (**4.57**). In the DC–AC inverter laboratory (**n = 24**), the overall mean was **4.37/5**. Item means were **4.54** for guide clarity, **4.42** for usefulness of the setup to understand converter operation, and **4.58** for added value compared with simulation. In the AC–AC laboratory (**n = 11**), the overall mean was **4.06/5**. Students reported **4.30** for clarity of explanations, **4.18** for overall lab quality, and **3.64** for the usefulness of the setup to consolidate knowledge. Open responses mentioned collective correction, the use of errors to guide improvement, requests for more time and more boards to work in parallel in AC–AC sessions, and hands-on confidence with PWM tuning and immediate oscilloscope feedback in DC–AC.

Table 1. Cohort-level means (overall and by laboratory)

Line	Mean	n	Notes
EBL methodology (global)	4.50	8	Survey methodology, Likert 1–5
DC–AC inverter lab	4.37	24	Survey module, Likert 1–5
AC–AC converter lab	4.06	11	Survey module, Likert 1–5

Table 2. DC–AC inverter lab—item-level

Item	Mean	SD	n	Missing
Guide clarity	4.54	0,72	24	0
Usefulness of the setup	4.42	0,97	24	0
Added value vs. simulation	4.58	0,65	24	0

Table 3. AC–AC converter lab—item-level descriptives

Item	Mean	SD	n	Missing
Clarity of explanations	4.30	1,25	10	1
Overall, lab quality	4.18	0,98	11	0
Usefulness to consolidate knowledge	3.64	1,63	11	0

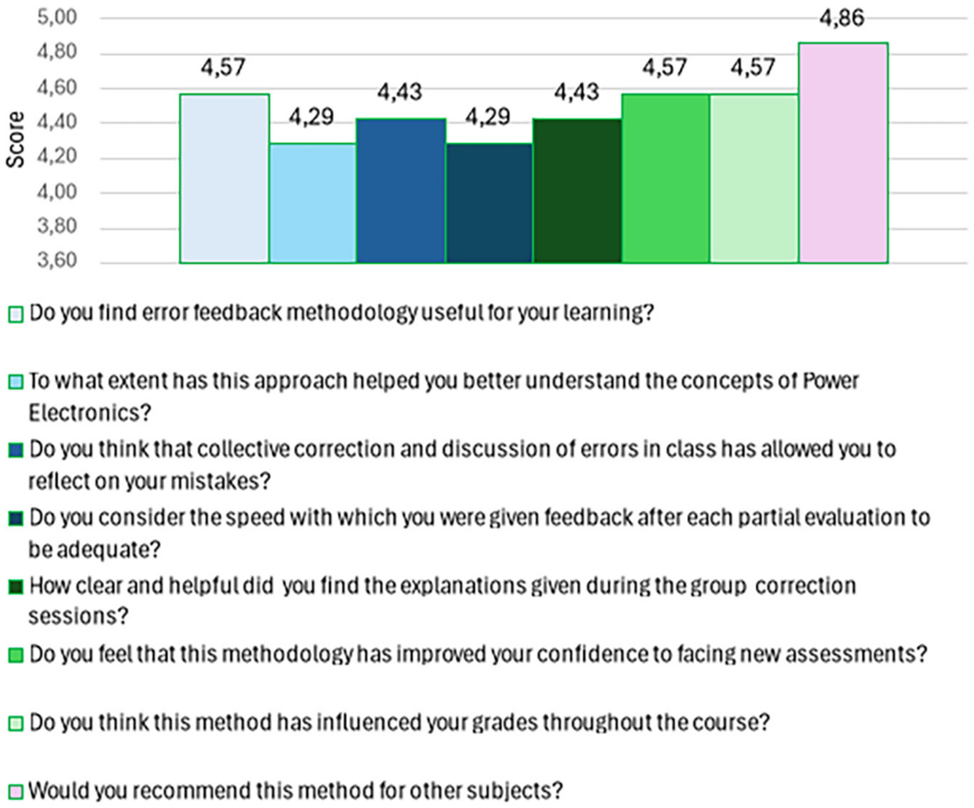

Fig. 3. Average results of the survey on the EBL methodology

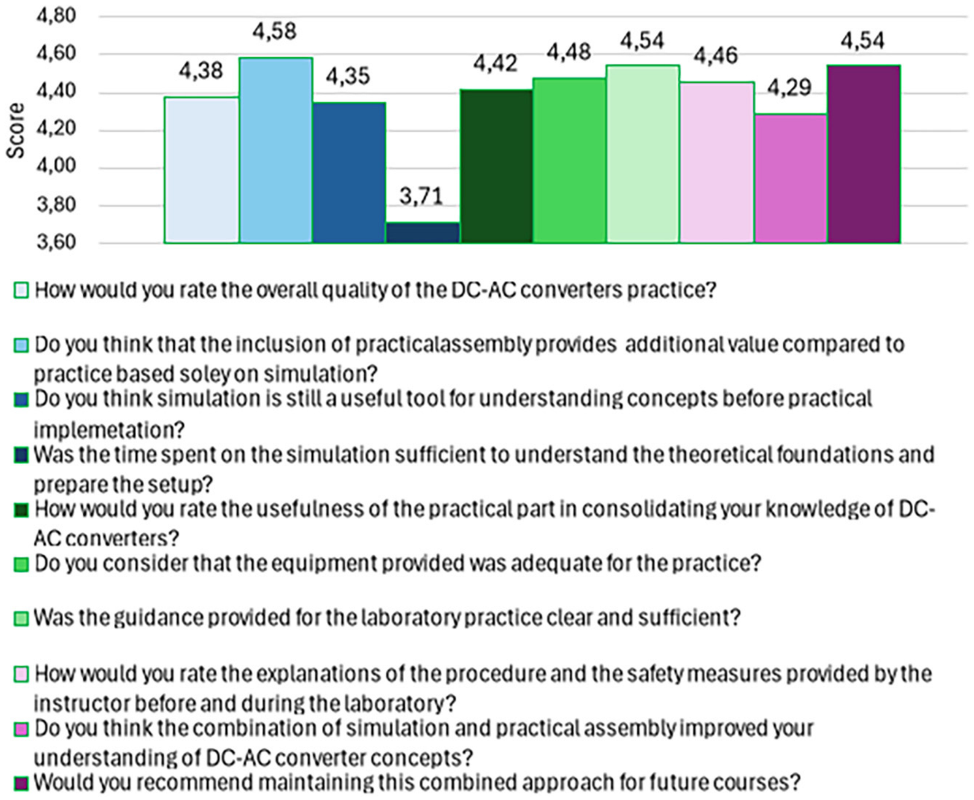

Fig. 4. Results of the DC–AC practice survey in a sample of 24 students

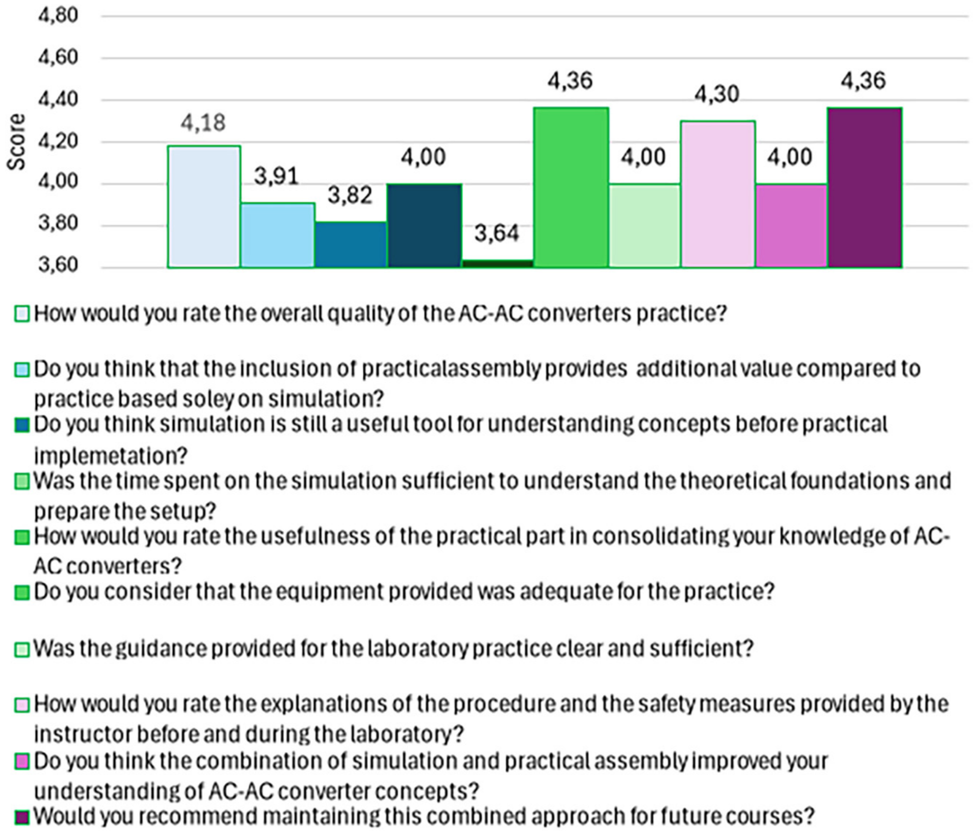

Fig. 5. Results of the AC–AC practice survey with a sample of 11 students

These outputs address the research questions stated in the Introduction. The cycle and the measures report how SRL is operationalized in postsecondary power-electronics labs. The cohort means provide indicators of perceived learning and error-handling efficacy. Parallel implementations in AC–AC and DC–AC offer comparative evidence for design choices in TEL laboratories.

6 DISCUSSION

This section interprets the findings in relation to prior theory and related work. It also presents implications, limitations, and future work.

Regarding feedback to SRL in TEL labs, the high EBL mean (4.50/5) and the strong item mean for confidence and recommendation are consistent with models in which formative feedback clarifies goals, progress, and next steps, and thus enables SRL cycles in authentic tasks [6]. Treating error as information fits the formative principles of criteria, comparison, and correction, and supports iterative improvement [7]. The emphasis on sustainable feedback helps explain positive signals in confidence and transfer between tasks [10].

Concerning AC–AC versus DC–AC patterns, the DC–AC line shows higher means for guide clarity and added value over simulation, while the AC–AC line shows a lower mean for knowledge consolidation. Viewed through task authenticity and instrumentation, DC–AC parameter tuning with immediate inspection in time and frequency may yield clearer error signatures and shorter feedback loops than multi-mode AC–AC commutation. This view aligns with studies linking well-instrumented and repeatable tasks with engagement and continuity [12] and with IoT-ready design principles that favor affordable hardware, accessible measurement, and structured logging [13].

In terms of value added relative to the state of the art, the design blends hands-on authenticity with instrumented traceability through oscilloscope use, FFT, THD, and parameter logs. This hybrid approach addresses a gap in SRL measurement by providing visible and timely signals that help students plan, monitor, and adjust [14]. The contrast between AC–AC and DC–AC supports design choices such as clear parameter-to-signal mappings, short pre-lab prediction tasks, and feedback prompts tied to observable error signatures.

For implications for practice, begin with prediction followed by observation to anchor feedback in explicit expectations, instrument each activity to make error signatures visible in time and frequency, use guiding prompts before solutions to preserve student agency, standardize parameter logs and screenshots to support reflection and replication, and reserve time for one guided re-attempt per session to close the loop.

As for limitations, the study relies on self-report scales and does not include objective performance indicators such as exam sub scores, error-rate reduction, or THD deltas. The single-institution, course-embedded context limits generalization. Time and equipment constraints can cap re-attempts, especially in multi-mode AC–AC sessions. These factors may influence the scores independently of the pedagogy.

Looking to future work, we will integrate objective analytics, extend method–result traceability with performance indicators, explore remote and IoT extensions to sustain practice beyond lab hours [13], and follow SRL subscales longitudinally to trace planning, monitoring and help-seeking in TEL contexts [14]. Multi-site replication is encouraged using the lab sheets in Appendix A and the bill of materials in Appendix C.

7 CONCLUSIONS

This study shows that placing errors at the center of technology-enhanced laboratory work is a viable way to foster active, reflective, and technically grounded learning in a power electronics course. The EBL design, coupled with short feedback loops and visible signal evidence (oscilloscope, FFT, THD), supported SRL processes and was well received by students. The cohort ratings were high for the overall methodology, and, in all implementations, the DC–AC line was considered more helpful than the AC–AC line. These findings are consistent with the intended contribution: operationalizing SRL through instrumented feedback cycles in higher education laboratories.

The approach adds value beyond prior active-learning experiences by making error signatures explicit and by structuring re-attempts. At the same time, the contrast between converter lines suggests that clarity in parameter-to-signal mapping and time for at least one guided re-attempt are pivotal for perceived learning. Together, the results support scalability and transferability to engineering subjects that blend theory and hands-on practice.

This work is directed at two audiences. For instructors and lab coordinators, the materials provided (lab sheets, traceability table, and bill of materials) enable replication and local adaptation. For researchers in TEL, SRL, and feedback, the dual implementation (AC–AC, DC–AC) offers a comparative testbed to study design choices that shape the learners' experience of error and feedback.

Limitations include the reliance on perception measures, a single institution setting, and time and equipment constraints that can limit the number of reattempts.

These boundaries frame the interpretation of the results and suggest caution in generalization.

Future work will focus on:

I. Integrating objective performance indicators (e.g., before or after THD deltas, error-type trajectories, targeted exam sub scores).
II. Extending the method: the result traceability with those indicators.
III. Exploring remote/IoT extensions to sustain practice beyond lab hours.
IV. Following SRL subscales longitudinally.

The authors intend to conduct these next steps in subsequent course iterations and invite the community to replicate and compare results using the shared appendices.

8 ACKNOWLEDGMENTS

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10 APPENDIX A—LAB SHEETS (AC–AC AND DC–AC)

10.1 AC–AC Conversion—Simulation Lab Sheet (common procedure for the five circuits)

Analyze the five modes in a single simulator (Multisim or LTspice). Record V_RMS and load power, list the first four FFT peaks in dB, and capture control and input/output waveforms. Use V1 = 10 V_RMS at 50 Hz, SCR 2N4174 (or equivalent), and the assigned R–L load. For each circuit, display I/O and SCR control, measure V_RMS and power, run the FFT in dB and note the four peaks, and then add one sentence that states the technical cause of the spectrum observed.

Circuit 1—Total regulation with phase control

Measurement	Value/Notes
Load RMS voltage (V)	
Load power (W)	
FFT—1st peak (dB)	
FFT—2nd peak (dB)	
FFT—3rd peak (dB)	
FFT—4th peak (dB)	
Comments on spectrum (technical causes)	

Circuit 2—Total regulation with cycle control

Measurement	Value/Notes
Load RMS voltage (V)	
Load power (W)	
FFT—1st peak (dB)	
FFT—2nd peak (dB)	
FFT—3rd peak (dB)	
FFT—4th peak (dB)	
Comments on spectrum (technical causes)	

Circuit 3—Differential regulation with phase control

Measurement	Value/Notes
Load RMS voltage (V)	
Load power (W)	
FFT—1st peak (dB)	
FFT—2nd peak (dB)	
FFT—3rd peak (dB)	
FFT—4th peak (dB)	
Comments on spectrum (technical causes)	

Circuit 4—Differential regulation with cycle control

Measurement	Value/Notes
Load RMS voltage (V)	
Load power (W)	
FFT—1st peak (dB)	
FFT—2nd peak (dB)	
FFT—3rd peak (dB)	
FFT—4th peak (dB)	
Comments on spectrum (technical causes)	

Circuit 5—Cycloconverter

Measurement	Value/Notes
Load RMS voltage (V)	
Load power (W)	
FFT—1st peak (dB)	
FFT—2nd peak (dB)	
FFT—3rd peak (dB)	
FFT—4th peak (dB)	
Comments on spectrum (technical causes)	

Comparative questions

- Compare Circuit 1 vs Circuit 2 in RMS and harmonic content. Explain.
- Compare Circuit 3 vs Circuit 4 in RMS and harmonic content. Explain.
- Which control type yields a higher harmonic content: phase or cycle? Why?
- Which circuit achieves the lowest THD? Provide evidence.

10.2 AC–AC Conversion—Assembly Lab Sheet (condensed operating notes)

Minimum instrumentation. Digital oscilloscope with rated probes (use differential for floating points), AC source as required by the board, True-RMS multimeter and AC–AC board.

Safety. Wire with the equipment off. Match load ratings. Double-check connections. Apply isolation where needed. Keep the emergency stop accessible.

Board operation. Use the *Menu* to select the mode, *Accept* to confirm, and *Change* to adjust the active parameter. Use a long press (≥1 s) to avoid accidental edits. Follow the connection table for total/differential regulation and cyclo-converter modes.

Per-mode measurements. Reuse the 10.1 table (I/O waveforms, V_RMS, FFT up to the 20th harmonic). Add a brief note on commutation artefacts.

Mode 1—Total regulation with phase control. Adjust firing angle between 5% and 95% in 5% steps (per half-cycle). For a 30% setting, perform:

Task	Record/Screenshot
Input and output waveforms	
Load RMS voltage (V)	
FFT spectrum up to 20th harmonic (dB)	

Mode 2—Total regulation with cycle control. Control via software: (a) number of inactive half-cycles (0–10), (b) number of active half-cycles (0–10). For 2 inactive and 2 active half-cycles, perform:

Task	Record/Screenshot
Input and output waveforms	
Load RMS voltage (V)	
FFT spectrum up to 20th harmonic (dB)	

Mode 3—Differential regulation with phase control. Repeat the measurement set and add notes on commutation and artefacts.

Task	Record/Screenshot
Input and output waveforms	
Load RMS voltage (V)	
FFT spectrum up to 20th harmonic (dB)	

Mode 4—Differential regulation with cycle control. Repeat the measurement set and add notes on commutation and artefacts.

Task	Record/Screenshot
Input and output waveforms	
Load RMS voltage (V)	
FFT spectrum up to 20th harmonic (dB)	

Mode 5—Cyclo-converter. Repeat the measurement set and add notes on commutation and artefacts.

Task	Record/Screenshot
Input and output waveforms	
Load RMS voltage (V)	
FFT spectrum up to 20th harmonic (dB)	

Summary table (AC–AC)

Mode	Key Parameter(s)	Load RMS (V)	FFT notes (artefacts up to 20th)	Comments
Total – phase				
Total – cycle				
Differential – phase				
Differential – cycle				
Cyclo-converter				

Deliverables (10.1–10.2). Submit simulation files 1–5, screenshots of I/O, control, and FFT, and a ≤1-page comparative summary of the five modes; for the assembly, add per-mode screenshots and notes plus a final comparative table.

10.3 DC–AC Inverter—Simulation and Assembly Lab Sheet

Simulate PWM-based DC–AC conversion and perform assembly on the didactic inverter PCB. Measure spectra and THD before/after the output filter and verify PWM timing relations.

Learning outcomes (as assessed)

- Analyze the inverter output as a function of input voltage.
- Study in frequency of the sinusoidal output generated by MOSFET switching (FFT and THD).
- Generate and analyze PWM control signals and relate duty to output level.

Materials and instrumentation

Item	Notes
PC with Multisim or LTspice	Simulate only in one program (choose one).
Digital oscilloscope + standard probes	Use cursors for pulse-width and amplitude; mobile phone photos only (no USB captures).
DC power supply	Recommended 12–18 V; NEVER exceed 18 V.
True-RMS multimeter	For RMS checks and supply monitoring.
Didactic DC–AC inverter PCB inactive DC–AC	Test points: PHx (phases), PWx (control), EN, and GND.

Safety and operating limits. Use 12–18 V DC and do not exceed 18 V. Verify wiring and probe category before powering on. Enable only after checks. Cut power before rewiring.

Part I—Simulation. Multisim route: sinusoidal modulator (4 Vpp, 2 V offset, 50 Hz), sawtooth carrier, comparator + NAND for complementary control, low-pass filter at output. The output level depends on source V3.

LTspice route: two 180° shifted modulators; behavioral sources for complementary control; drivers such as VCVS (24 V); voltage-controlled switches; low-pass filter; output varies with V1.

Simulation activities

Quantity	V3 = 2 V	V3 = 11 V	Notes/Screenshot
Frequency (Hz)			
Peak-to-peak voltage (Vpp)			
Minimum voltage (Vmin, V)			
Mean voltage (Vavg, V)			
RMS voltage (Vrms, V)			

Harmonic analysis and THD (V3 = 11 V)

Harmonic	Amplitude Before Filter	Amplitude After Filter
1		
…		
10		
THD before filter	THD after filter	Comments

PWM timing analysis (V3 = 11 V)

Condition	Pulse Width (ms/us)	Duty (%)	Notes/Screenshot
Output at the mean			
Output at maximum			

Part II—Assembly

Test points and use

TP	Function/What to measure
PH1, PH2, PH3	Unfiltered phase outputs R, S, T (observe switching artefacts).
PW1, PW2, PW3	MOSFET control signals for phases R, S, T (timing/duty checks).
EN	Enable signal (activate output).
GND	Reference ground for all measurements.

Assembly activities

1. Set output amplitude to 10% at 50 Hz; measure frequency, Vpp, Vrms, and Vavg.
2. Repeat at 90% amplitude and 50 Hz.
3. Set amplitude to 50% and 50 Hz; measure pre- and post-filter spectra (first 10 harmonics) and compute THD; discuss.
4. Repeat harmonic measurement at 100 Hz.
5. With amplitude at 50% and 50 Hz, display the filtered output and its control signal.
6. Measure PWM pulse width when the output is at its mean value and at its maximum (use cursors).

Measurement tables—50 Hz

Amplitude	Frequency (Hz)	Vpp (V)	Vrms (V)	Vavg (V)	Screenshot
10%					
90%					

Harmonic tables—50 Hz, 50% amplitude

Harmonic	Pre-filter Amplitude	Post-filter Amplitude
1		
…		
10		
THD pre-filter	THD post-filter	Comments

Harmonic tables—100 Hz, 50% amplitude

Harmonic	Pre-filter Amplitude	Post-filter Amplitude
1		
…		
10		
THD pre-filter	THD post-filter	Comments

Control overlay and timing (50 Hz, 50% amplitude)

Overlay Shown (Y/N)	Pulse Width at Mean	Pulse Width at Max	Notes/Screenshot

Evidence policy and deliverables. Provide oscilloscope photos, simulation files, and a PDF with key results (RMS/Mean/Vpp, spectra pre/post filter, THD, and PWM timing). Package as a ZIP: P5_surname.

Acceptance criteria

Criterion	Target	Met (Y/N)
The output fundamental matches the modulator frequency	Yes	
RMS/mean values consistent with the amplitude setting	Yes	
THD decreases after filtering (50 Hz, 50% amplitude)	THD_post < THD_pre	
The PWM duty/time aligns with the output level	Consistent	
Screenshots and parameter annotations present	Yes	

Data capture checklist

- Photos of waveforms and spectra
- Parameter logs (V3, amplitude %, frequency)
- CSV/images of FFT/THD
- Notes uploaded to the LMS

Reflection prompts (SRL)

- Which change in duty had the largest effect on Vrms? Why?
- How does the filter alter the first ten harmonics and THD?
- What would you change next time to reach targets faster or with fewer errors?

11 APPENDIX B—METHOD → RESULT TRACEABILITY

Method Element	Operationalization	Data/Artefacts	Linked Result Variable	Analysis Link	Expected Direction	Validity Threats & Mitigations
Formative evaluation (Step 1)	Diagnostic micro-tasks; error pattern review	Item scores; error types	Clarity of goals; preparedness	Descriptives; mapping	↑ clarity; fewer conceptual errors	Rubric + exemplars
System manipulation (Step 2)	Board setup; change firing angle/PWM	Parameter log; photos	Authenticity; confidence	Completion of the checklist	authenticity ↑ authenticity; ↑ confidence	Standard sheets; peer check
Measurement	Oscilloscope; FFT; THD	CSV; snapshots	Technical understanding	Exemplar matching	↑ understanding	Calibration
Diagnosis	Observed vs expected; causes	Annotated plots	Efficiency of Error-handling	Thematic coding	↑ efficacy	Time-stamped notes
Scaffolded feedback (Step 3)	Guiding questions	Feedback logs	Feedback clarity/ timeliness	Survey items; effect sizes	↑ quality; ↑ timeliness	Prompt templates
Re-attempt (Step 4)	Adjust; repeat	Before/ after; THD Δ	Improvement index; persistence	Wilcoxon; Cliff's δ	↑ improvement	Note incomplete loops

12 APPENDIX C—BILL OF MATERIALS (GENERIC)

Item	Spec/Notes	Qty	Acceptable Alternatives/Ranges
Microcontroller control board	32-bit MCU; ≥160 MHz; 2+ timers; PWM; UART/USB; ≥20 GPIO	1/station	ESP32/STM32 class
AC–AC educational board	TRIAC/SCR stage; isolated drivers; multiple modes	1	Any didactic AC–AC kit
DC–AC inverter board	Full-bridge; PWM input; heat-sunk switches	1	MOSFET/IGBT stage
Digital oscilloscope	≥100 MHz; ≥1 GSa/s; 2+ ch; USB export	1	70–200 MHz

13 AUTHORS

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