Integrated Circuits Testing: Remote Access to Test Equipment for Labs and Engineering

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***Abstract*—This paper concerns the local and remote use of an Integrated Circuits (IC) Automated Test Equipment (ATE) for both educational and engineering purposes. This experience was initiated in 1998 in the context of a French network (CNFM) in order to provide a distant control to industrial equipment for academic and industrial people. The actual shared resource is a Verigy V93K System on Chip (SoC) tester platform. The cost of such an equipment is close to 1M€, without taking into account the maintenance and attached human resources expenses to make it work properly daily. Although the sharing of this equipment seems to be obvious for education, the French experience is quite a unique example in the world. Here, practical information regarding IC testing and network setup for remote access are detailed, together with the associated training program.**

***Index Terms*—Automated Test Equipment, IC Testing, Remote Labs, Education, Network.**

I. INTRODUCTION

This paper introduces the French experience of distant education and engineering in the field of Integrated Circuit (IC) testing based on the remote access to unique and up-to-date test equipment. At the national level, early attempts to spread low-cost machines among several universities failed to obtain good results. The reasons were that first, low-cost testers do not represent the industry reality so that getting experienced on those machines does not provide strong added value; and second, developing training modules and labs in the field of IC testing, and providing support for engineering requires good technical support and staff with high degree of expertise which is not easy to find. Finally, the maintenance constraint was too high and equipments were turned off, one after one.

The National Test Resource Center of CNFM (so-called CRTC) has been created to answer to the industrial demand in engineering curriculum with Design & Test competences. The CNFM (Comité National pour la Formation en Microélectronique) is a public organization that federates academic and industrial partners for the purpose of education in Micro and Nano-electronics [1]. CNFM focuses on making heavy educational resources such as professional CAD tools, clean rooms, or industrial test equipments available for common use, by all French universities and industrial partners. Considering the huge cost of up-to-date IC testers, the policy of CNFM was to setup a single test center for all the French academic centers. So in 1998, the University of Montpellier was chosen to host and develop the CRTC activity. The technical platform benefits from the competence of more than 25 people (researchers and professors) from a research laboratory (LIRMM [2]) internationally renowned in the field of design and test of integrated circuits and systems. Research projects include DFT and BIST for digital, analog and mixed-signal circuits and design and test of integrated MEMS. In addition, the CRTC team includes a test engineer who manages all the technical support to users and develops training materials.

To avoid any excessive travel expense for users, the implementation has been designed to make the CRTC equipment reachable from any remote center [3]. For about ten years, CRTC has provided support in IC testing, based on the remote control of industrial test equipment. On a national level, more than 100 students and engineers per year have been trained using this support from 1998 till now. In 2003, after a 2-year long European IST (Information Society Technology) project was completed, users from Germany, Spain, Italy and Slovenia were able to take control of the tester for remote engineering [4]. Figure 1 shows the European coverage of CRTC services after 2003.

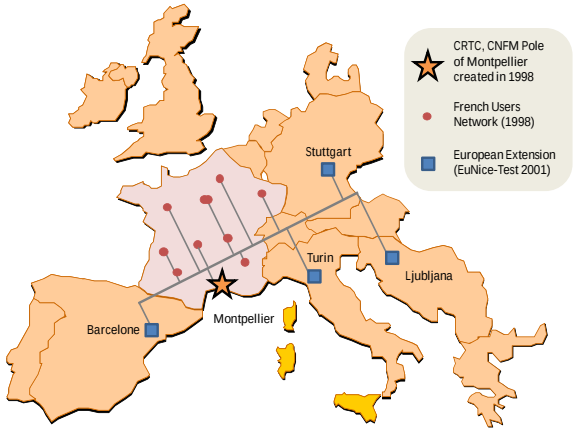


Figure 1. CRTC localization and users network in France and Europe

The paper is organized as follows: section 2 introduces the context of Integrated Circuits testing and its specificities from the industrial point of view. The cost of the equipment is addressed to demonstrate the interest of a shared platform. Section 3 details the CRTC platform setup in terms of available hardware and associated network configuration to make easy the remote access and the distant learning with interactive support from a teacher. Section 4 provides information regarding the training modules developed at CRTC in order to address educational needs ranging from undergraduate level to

Ph.D. students. Finally, section 5 goes into the technical details of preparing an industrial test program, in order to give a more precise feeling of the matter.

II. CONTEXT OF IC TESTING

A. IC Manufacturing

Manufacturing test of Integrated Circuits consists in verifying the quality of a product with respect to its specifications. For most of the manufactured products the cost of the final verification represents only a small part of the production costs. This is due to the fact that these products are either high cost (e.g. automotive industry) or reliable enough to authorize randomly applied verification (e.g. food industry). This scheme doesn't apply in the microelectronics industry where low cost products may be produced with a significant number of out-of-specification or non-functioning parts. Manufacturing tests are then required to verify the physical integrity and the correct behavior of any produced parts at a reasonable cost. The problem is that manufacturing test introduces a breakage in the batch fabrication concept. Indeed, speaking about malfunctions leads to singularities that cannot be dealt in a batch-based model. Even if test is undertaken at the wafer level and if parallelism is still possible each produced device must be tested independently to discard the few percent of defective circuits [5].

Figure 2 illustrates the global strategy of cost reduction in IC manufacturing. Roughly, the total fabrication cost comes as a sum of expenses related to the silicon processing, the packaging and the test. In each case strong efforts are made to achieve cost reduction: Silicon cost are reduced by increasing the integration capability though smaller devices and higher production volumes, taking benefit from the batch fabrication approach; packaging cost are addressed by reducing both package sizes and the pin count. Finally, test costs are lowered by reducing the amount of required test data to transfer, by testing several circuits in parallel (multi-site testing) and by shortening the test time. Obviously, all these attempts to save money require skilled people in very specific domains.

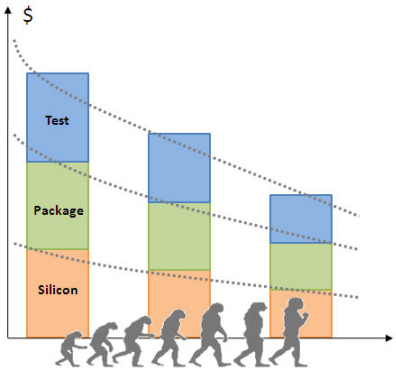


Figure 2. Evolution theory applied to the test cost in IC manufacturing

B. Cost of the ATE

The testing of Integrated Circuits is done in highly automated test environment based on so-called Automated Test Equipments (ATE) which will be further described in following sections. An ATE is a flexible platform that can host various hardware resources depending on the requirements of the circuit to be tested. Commonly, an ATE includes digital channels that write to and read from digital pins of the circuit under test and dedicated channels for the device supply. In more advanced configurations, analog or even RF channels are available.

The cost of an ATE therefore depends on the number and the type of channels being hosted in the machine. It comes:

$$ATE\_Cost = B\sum_{n}(m \times x)$$

Where B is the base cost of the ATE, m is the cost of a channel and x the number of channels. Table I gives examples of ATE costs in k€ for various classes of integrated circuits which strongly differ in terms of pin nature and pin count [6].

TABLE I.
ATE COSTS DEPENDING ON PRODUCTS UNDER TEST

Product	B	m	x
	Base Cost (k€)	Cost per pin (k€)	Number of pins
Microprocessors	250-400	2.7 to 6	512
Mixed-signal (e.g. audio)	250-350	3 to 18	128/192
Microcontroller	200-350	1.2 to 2.5	256/1024
Memory	200	1	1024
RF	200	50	32

In the industry, ATE are running 24 hours so that time slots for development and training are somewhat difficult to find. In this context, CRTC provides a unique opportunity to get access to those expensive test equipments for both education and engineering purposes.

C. Production Test versus Characterization Test

Commonly, testing a circuit consists in verifying its behavior (its functionality) for all possible input situations. For digital circuits, this is called exhaustive testing. Practically, functional testing of digital circuits having few tens of inputs is not possible because it would take too much time, even with state-of-the-art ATE. For this reason, the functional test is replaced by something called structural testing which consists in applying a reduced number of input combinations in order to verify the integrity of the component according to a predetermined fault list. The fault list is built after a fault model. A common fault model for digital circuits considers that each net of a circuit can be stuck at a given logic state (0 or 1). For years, this model has been used in CAD tools to automatically generate test patterns after the circuit netlist. For analog or mixed-signal circuits, functional testing is still considered due to the continuous nature of signals. In this case, circuit specifications are directly verified (i.e. gain, bandwidth, offset, linearity…) after digital processing of the circuit response.

In the industrial context, two distinct kinds of test are performed: characterization test and production test. The characterization test is performed first, after early dies are produced. The objective is of course to verify the device functionality but more especially to measure the circuit performance in order to determine all the specification that will appear in the component datasheet. It concerns static (DC) parameters such as output voltages, current capability, input levels, leakage, and dynamic (AC) parameters such as propagation delays, setup and hold times, operating frequency, etc. The characterization test is not under strong timing constraint (a few minutes is acceptable). It

must provide accurate information and statistical data in order to determine, for each parameter of the datasheet, a range of acceptable values. Note that the datasheet is a contractual document which states the guarantied performances.

The production test has no other purpose than verifying that manufactured circuits meet the datasheet. Because production test is performed on every single product, it has to be very fast (a few seconds). Basically, a production test consists in a flow-chart implementation of elementary tests (*Test Flow*), each having a simple Pass/Fail output (see Fig. 3). Doing so, it is possible to distinguish the failure origin and to perform a sorting (*binning*) for both good and bad circuits. For instance, this approach is used to sort processors by operating frequencies. The production test is considered right after foundry at the wafer level (*wafer sort*) and after packaging (*final test*).

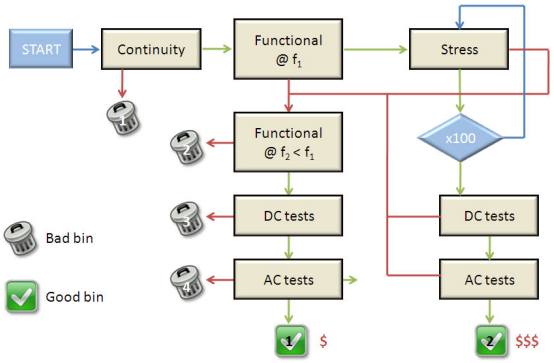


Figure 3. Test flow example with two "good bins" to sort devices depending on their performance.

III. CRTC HARDWARE AND SOFTWARE SETUP

The CRTC platform has been sized to respond to the academic and industrial demand in terms of education and engineering. The ATE model has therefore been chosen to allow flexibility regarding circuits to be tested while network configuration is designed to simplify software installation for distant users.

A. Test Equipment

The CRTC tester is a V93K model from Verigy®. Verigy is one of the four major test equipment manufacturers in the world and is well represented in the European microelectronic industry, which is an essential concern regarding education. The V93K platform targets SoC (*System-on-Chip*) products (i.e. Digital, Mixed Signal, RF, embedded memory, etc.) testing. It is made of a test head that can host various resources such as digital channels, analog sources and digitizers, supply or RF boards. The user is therefore able to optimize the configuration to meet the Device Under Test (DUT) requirements. Figure 3 illustrates the basic elements that compose the ATE available at CRTC. The main part is the testhead. This testhead is a compact model dedicated to engineering (i.e. development of test programs) and trainings. It can host up to 18 boards (Pin Electronics) for a maximum number of 512 digital pins based on the available 32-channels boards. Programming is performed using a regular computer running dedicated software under Linux. The communication between the testhead and the computer is an optical GPIB link.

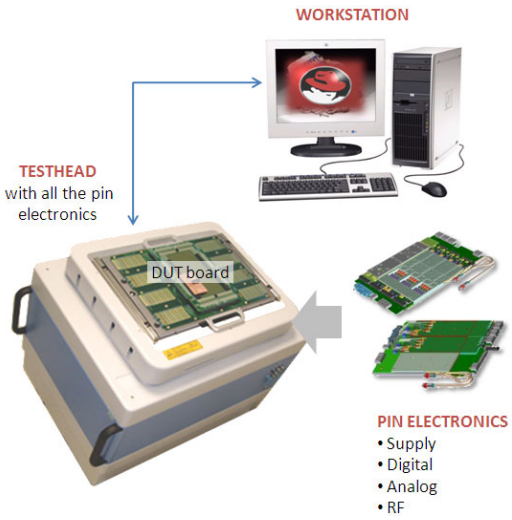


Figure 4. Main Hardware Components of an ATE

At that time, the testhead is equipped with supply, digital, and mixed signal resources as summarized in table II. This setup allows CRTC to address both digital and mixed signal testing. Memory testing is also possible without additional resources. In most cases, the devices under test used for training are not too complex for obvious educational reasons. Regarding the performances of the boards, the PS3600 features digital channel with sampling rates up to 3.6GSps, which are suitable to test state-of-the-art very high speed digital circuits. The PS800 provides an additional 32 digital channels for general purpose use. The AV8 board is designed for current multimedia circuits with both audio/video resolution and bandwidth. Finally, 16 independent supplies are available, which is more than enough in most cases.

TABLE II.
CRTC HARDWARE RESSOURCES (PIN ELECTRONICS)

Board	Type	Qt	Channels / Board	Specs
PS3600	Digital	1	32	3.6GSps 64Mvec Memory
PS800	Digital	1	32	800MSps 64Mvec Memory
AV8	Mixed Signal	1	8	24bits / 200kSps 14bits / 65MSps
MSDPS	Supply	2	8	-8V to 8V / 2A

B. Software Setup and Tester Virtualization

The test program is developed into an environment called SmarTest®, which is based on the open platform Eclipse® shown in figure 5.

The application manages the various setup files (pins, levels, timing, and vectors) and is used to build testflows. SmartTest comes with a library of pre-programmed basic test functions for all the essential operations: functional test, continuity test, DC or AC parameter measurement, etc. These test functions are very helpful for beginners. For advanced users, custom test functions (also called Test Methods) can be programmed directly in C, compiled and built into the same environment.

The software/hardware interaction is built upon the concept of "live-machine". When programming through

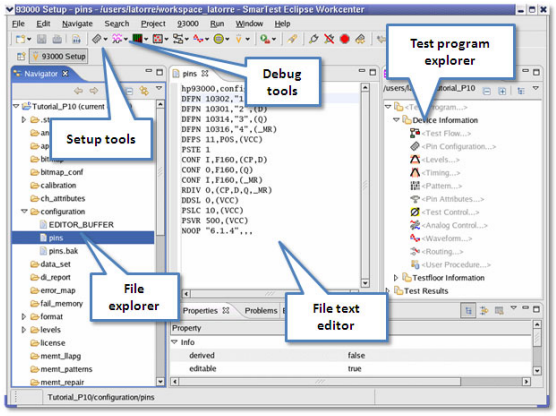


Figure 5. Smartest® programming environment based on Eclipse® IDE

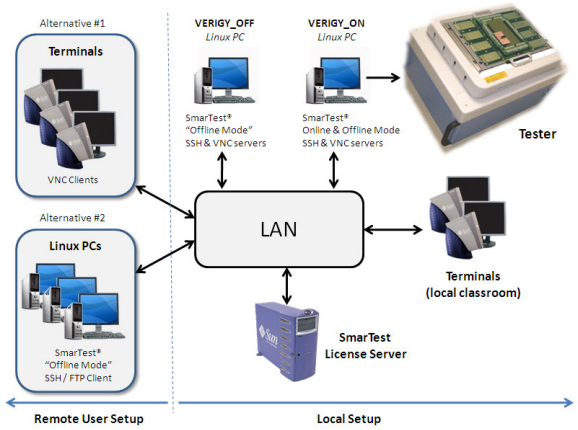


Figure 6. CRTC Network Setup for local and remote control of the ATE

software, data in the tester memory is continuously updated. In others terms, software windows are like views of the tester memory content in real time. This speeds up the program development and debug as there is no need for compilation or download steps. The counterpart of this interaction scheme is that the software needs the physical tester to operate. For parallel use in the context of a classroom, the hardware is not divisible and it would lead to a dead end without the availability of an "offline" mode.

In "offline" mode, the tester hardware is emulated in software so that SmarTest operates just the same as in online mode as long as no real test result is expected. This virtual tester can be duplicated as much as desired so that it is possible to run several SmarTest sessions in parallel, which is a Sine qua non condition in a classroom context.

CPU requirement to run Smartest is not an issue as it is mainly a capture tool. The amount of required RAM depends on the number of offline sessions to be run in parallel but does not exceed today's regular desktops configurations.

C. *Network Setup*

The network setup has been designed to allow the maximum level of flexibility for distant users. Locally, the SmarTest software is hosted by two Linux computers, namely VERIGY_ON and VERIGY_OFF. The first one is physically connected to the tester and is dedicated to online sessions. At some point in the development, each user will connect to this computer to run its test program on the real device. The second one runs SmarTest in offline mode only, and is intended to support the multisession development phase.

Distant users have two options, depending whether they want to install and run SmarTest locally or not. The recommended option (Alternative #1 in figure 6) is to connect directly to CRTC Linux stations using a VNC (Virtual Network Computing) client, the same way it is done in the local setup of Montpellier. VNC clients are lightweight software, freely available for all kinds of operating systems, turning any computer into a VNC terminal. There are no other requirements regarding software installation and license checking is totally transparent for the user since SmarTest runs on CRTC stations.

As VNC technology is a remote desktop approach, it may suffer from Internet latency, although it is not really an issue with today's Internet bandwidth. Anyway, a solution to improve the interactivity with SmartTest is to proceed to a local installation. In that case, the network connection is only required for license checking (Alternative #2 in figure 6).

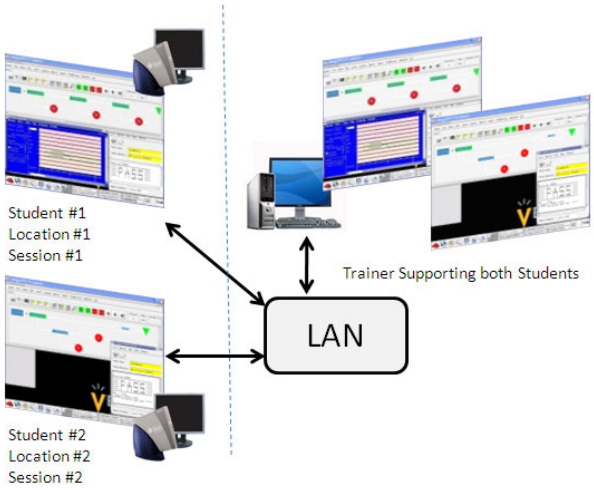


Figure 7. Illustration of distant support using a VNC client/server configuration

VNC technology offers an easy way for the distant access to the tester. Besides, there is another reason to promote this approach in the context of distant learning: the same desktop can be shared between users. This capability brings a lot of interactivity between students and teacher. Indeed, the teacher desktop can be seen by the students, allowing live demos to be performed. Also, the teacher can see and take control over any student desktop to contextually bring help where needed (figure 7). Coupled with a VoIP (Voice over IP) solution, a virtual classroom can be experienced with trainer and trainees spread anywhere.

IV. TRAINING CONTENT

The CRTC primary objective is to support educational programs (both initial and continuing) through practical courses and labs. Beside, CRTC offers access to the tester for engineering. This section focuses on professional training programs.

The usual way to work with distant users is to organize first training for trainers in Montpellier. The second step is

to help the distant trainer to setup the connection from its place. After that, each trainer is free to place a reservation for the tester by checking its availability on CRTC web site [7].

The manner each training course is implemented depends on the local context. The global organization of syllabus, the initial level of the trainees and the pedagogical approach of the teaching team make the organization different in terms of number of attendees, number of groups and course duration. This demonstrates the good flexibility of the remote system. Once a working time slot is booked, the tester is fully devoted to the remote center. Then the teacher can use the tester, exactly as if it was located on the local site, and he can implement the training at his own convenience.

Because CRTC remains first user of the tester, we develop and disseminate training material. In the past years, most of the training modules were based on Verigy's professional educational material, which are mainly developed for test engineers, and so are focusing more on the ATE operation than on testing fundamentals. Today, we have identified three educational levels where industrial testing may be of special interest if addressed relevantly. At undergraduate level (L), only digital circuits are addressed with emphasis on device characterization and datasheet related aspects. At graduate and engineering level (M), modules are sized to provide a real professional experience of the tester usage. Both digital and mixed signal devices are concerned. Finally, at Ph.D. level (D), advanced techniques such as custom test function coding can be addressed.

A. Undergraduate Level

At undergraduate level, students are using electronic components daily, and have become familiar with their datasheet without having any idea on how this latter has been constructed. As the only prerequisites for testing a standard IC are the basics of fundamental electronics, we can go through the development of a complete test program. During the training, students often rediscover the role of the circuit datasheet. As an example, a majority of students completely ignore the importance of critical parameters such as setup time and hold time for the good design of sequential circuits. The lab part of the training is the occasion for them to visualize and measure these timing parameters. More generally, the proposed training module aims at providing an in depth exploration of the datasheet for a simple digital circuit from the TTL logic family.

B. Graduate Level

Digital training courses aim to initiate students and engineers to digital IC test. After completing a digital training, each trainee will be able to (i) make competent use of any digital ATE to test a device for its performance parameters and specifications, (ii) build up a test flow to automate the test execution and (iii) create a test program to be executed on the production test floor. The training courses use a standard digital circuit as DUT to simply illustrate all the test functions. Each training course is built up on lessons and related lab exercises. Table III shows typical agenda for 4 days digital training.

Mixed-signal training courses introduce the test of analog and mixed-signal circuits. After completing the training, students are able to make competent use of the tester to test both ADC and DAC device for its performance, parameters and specifications. They are prepared to plan appropriate tests by utilizing the DSP instruments. Fundamentals of analog testing are addressed, with focus on analog circuit characteristics such as linearity, gain, offset, etc.

TABLE III.
DIGITAL TRAINING TYPICAL AGENDA

Day	Program
1	Tester HW/SW overview Test program development: Pin configuration, level, timing, Pattern Continuity and Functional tests implementation Test flow
2	Test execution and Result analysis: Datalogging Debugging tools
3	Characterization tests : AC tests: Vil/Vih, Vol/Voh, leakage DC tests: set up hold, propagation delay times Shmoo plots
4	Advanced test features: Global variables Pin Margin, Histogram Burst mode Preparation to mixed-signal training: Test methods

C. Continuous Education & Research

As the CRTC is a Verigy's backup training center since February 2008, test trainings are also delivered to industrial people. They require Verigy's agreement and are done using Verigy's policy and training materials.

The CRTC trainer is a Verigy certified trainer who also has 10 years experience in test engineering. The trainer is skilled in digital, mixed-signal and memory tests which allow CRTC to offer a large range of test services. Test trainings are executed based on a predefined planning or on demand according to trainer's availability.

In addition to the training program, the CRTC platform also supports various educational and research projects:

- In collaboration with University of Strasbourg: A teaching project concerns the design and test of a full mixed-signal ASIC with application to magnetic field sensing. CRTC is in charge of developing labs on test vectors automatic generation and test implementation on ATE.
- In collaboration with Verigy: CRTC provides support to a research project concerning the test of RF circuits using high-speed digital channels and specific algorithms.
- Internal project: CRTC develops new labs allowing the user to customize the DUT using an FPGA. This offers opportunity to have virtually any kind of logic function and to synthesize faulty behavior (static or dynamic faults) in order to introduce diagnosis considerations in the labs.

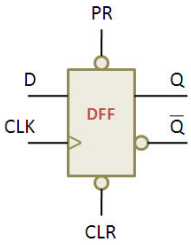
According to the online reservation status, the tester usage reaches 80% of working hours for the first quarter 2009 (for both education and research).

V. TEST PROGRAM DEVELOPMENT

The purpose of this section is to give an overview of a test program implementation taking for example a simple digital device. Basically, testing a device consists in applying electrical signals to its inputs and measuring response from its outputs. Practically, many parameters have to be defined such as the voltage levels, the timings, the sequence of input vectors, the nature of the measurements, etc.

In order to illustrate the programming steps, let us consider the case of a flip-flop cell shown in figure 8, which can be considered as the simplest existing sequential digital circuit as it only propagates and memorizes on pin 'Q' the value ('0' or '1') applied on pin 'D' after a rising edge of the clock on pin 'CLK'.

To build a test program, the preliminary work is to create a setup for a functional test. This setup is based on four steps: the pin definition, the level and timing configuration and the test data (pattern) edition. This flow is depicted in figure 9.



Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$ 0

Figure 8. A simple flip flop device as a case study for a digital test program development

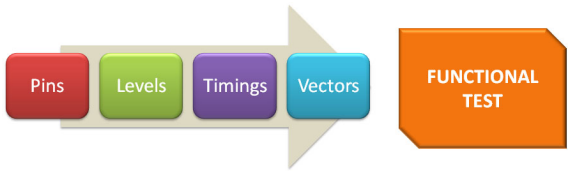


Figure 9. Basic steps to setup a Test Program for a digital circuit

A. Step 1 : Defining the Pins

The pin definition simply tells the software which tester channels are connected to which circuit pins. For each pin of the circuit under test, a name is given and attached to a single tester channel address. The nature of the pin (input, output, input/output, supply, etc) is given here.

Groups of pins are also defined here in order to simplify the subsequent programming. For instance, several pins having the same level or timing parameters may be grouped together to improve the development efficiency.

The ATE electronics is built on a per-pin architecture which means that every single pin (or channel) has its own hardware resources for storing setup parameters (memory) and running the test program (test processor). Allocating a tester channel to a pin thus determines which hardware resources will be used for that pin. Moving a pin from one tester channel to another then implies a transfer of all stored information from one physical memory to another and must be handled carefully.

B. Step 2 : Defining the Levels & Timings

Figure 10 illustrates the electronic architecture of a tester channel for a digital pin, which can be an input, an output or an input/output. The test sequence is under the control of the test processor. Signal sent to and received from the device under test are generated by means of a vector memory which selects, time after time, the appropriate signal shapes stored in the waveform memory. Precise timings are obtained using a timing generator while levels (voltages and currents) are determined in the driver and comparator stages.

In addition, a programmable measurement unit (PMU) can be connected to the device pin to execute precise voltage measurement under current loading, or precise current measurement under voltage loading. This unit is mainly used to verify the static (DC) parameters of the circuit (output voltages, input leakages, etc…).

The main settings for each digital channel concern:

- The levels: Signals are applied to the device under test using the driver D which converts logic '0' and '1' into real voltages. In return, signal coming from the device are converted into logic states by the comparator C based on programmable detection thresholds. Figure 11 details the comparator architecture and the parametric load circuit. Associated parameters are V_{OH} and V_{OL}, the two thresholds used to determine if the output voltage coming from the DUT is assumed to be a '1' (greater than VOH), a '0' (lower than VOL) or undetermined (in between). In addition, current load can be applied to the device output using the parametric load (PL) for each state (I_{OH} and I_{OL}). Termination (V_T) and clamping voltages ($V_{clp}H$, $V_{clp}L$) may also be programmed.
- The timings: Driver and comparator events are first defined as waveforms with no timing information and stored in the wavetable. The timing generator then locates each event in time. This separation allows using the same set of waveforms with different timings. In the programming formalism, a "write" event is named 'd' (for drive), while comparator is triggered by a 'r' event. (for "receive"). Events are also called "edges".

Figure 12 shows the chronograms for a simple functional test of the flip-flop device. It is based on two clock periods used to verify the correct propagation of both '0' and '1' value through the latch. From this example, the timing definition for the 'D' pin is established. Two waveforms are stored in the waveform memory associated with the pin 'D', with only one timing parameter (t_1) which is used to trig the "write" event, at the beginning of each sequencer period.

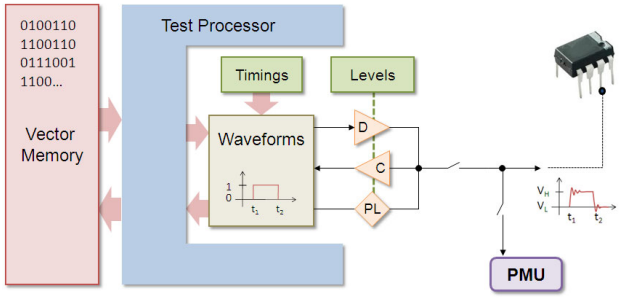


Figure 10. Schematic view of a digital channel connected to a device I/O

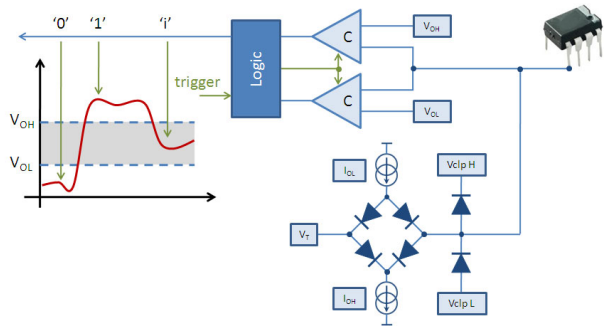


Figure 11. Details of the comparator bloc (C) and parametric load (PL) with associated parameters to setup for the capture of digital outputs

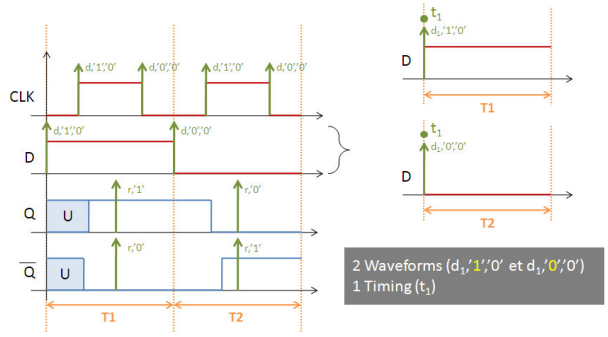


Figure 12. Example of Timing definition for the pin 'D' of the flip flop latch

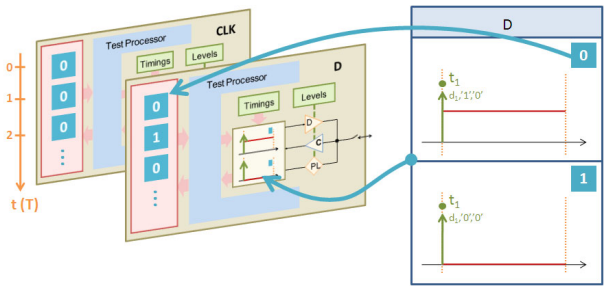


Figure 13. Definition of the vector table

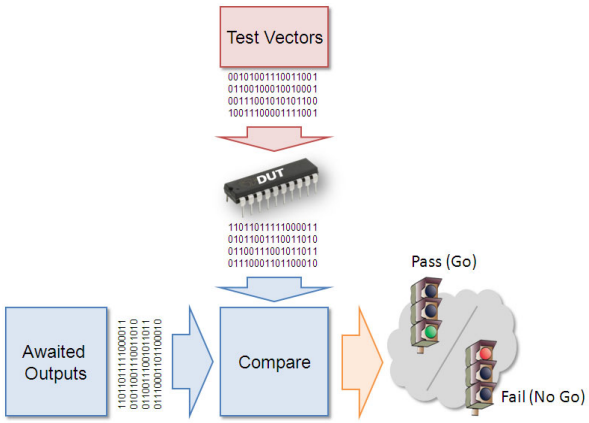


Figure 14. Illustration of the functional test

C. *Step 3 : Defining the Vectors*

The vectors represent the data transferred between the ATE and the device under test during the test execution. Practically, it is a table where each column corresponds to a pin, and each line corresponds to a sequencer period. The values stored in this table are actually pointers to waveforms. Following the previous example, figure 13 shows that two waveforms are stored in the waveform memory of pin 'D'. The vector memory then calls sequentially the waveform of index '0' and the waveform of index '1'.

The vector setup determines the sequence of test patterns to be sent to the circuit and is therefore critical for the test quality. In most real cases, it is impractical to test a device exhaustively because it would take too long to apply all possible combinations. Software such as an Automatic Test Pattern Generator (ATPG) is then used to create optimized sequences that cover a maximum number of possible defects. Nevertheless, the sequence programmed in the vector table can be used in the context of several measurements, including the verification of voltage levels, timings, etc. For this reason, it must be programmed with caution, making sure for instance that for a simple functional test each pin toggles from '0' to '1' and inversely at least once during the sequence.

D. *Step 4 : Debugging the Functional Test*

The last step of the setup is to run and debug the functional test. As shown in figure 14, a functional test simply consists in applying the test patterns as defined in the vector setup. If the awaited data corresponds to the actual output from the device under test, the result is "Pass". Otherwise, the result is "Fail".

When the functional test fails to succeed, the software environment provides tools to help tracking errors. For example, an "error map" shows at which cycle, and for which pin an unexpected result occurred. If necessary, the ATE can repeat the functional test while sweeping level and timing parameters. This technique is used to rebuild the analog shape of received waveforms and is a very powerful debug tool.

VI. CONCLUSION

In this paper, the quite unique French experience (CRTC) of sharing heavy test equipment for education and engineering is detailed. Because of the cost of such equipment in terms of both initial investment and required skilled staff for daily operation, the benefit of distant access is obvious. The use of emerging virtual computing solutions greatly improves the interactivity between distant users and local teacher as virtual desktops can be shared.

Educational modules have been developed to address various needs, from undergraduate to Ph.D levels and to bridge the gap between the academic approach of IC testing and the industrial demand. Today the CRTC service is used both locally and remotely by about 100 students each year at the national level.

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