A Sequential Logic iLab Utilizing NI ELVIS II+ and the Interactive iLab Architecture

http://dx.doi.org/10.3991/ijoe.v8i3.2114

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***Abstract*—Recent trends in development and utilization of online laboratories have resulted into standard platforms that are not lab-specific, which can be leveraged to develop laboratories in diverse fields. One such platform is the Massachusetts Institute of Technology (MIT) interactive iLab Shared Architecture. This paper presents work undertaken at Makerere University to develop a synchronous sequential logic iLab based on this architecture. The research was carried out by a Graduate researcher, under joint supervision in the confines of the iLab Africa Graduate Fellowship Programme. The research builds on previous work undertaken by the same researcher, in which a combinational digital logic iLab was developed. The sequential logic iLab utilizes the National Instruments Educational Laboratory Virtual Instrumentation Suite (NI ELVIS II+) hardware, with its interactive user interface developed using the Laboratory Virtual Instrument Engineering Workbench (LabVIEW). The generic platform supports experiments in the fields of counters, shift registers, frequency dividers and digital clocks, with appropriate electronic component selection and configuration. The design methodologies and implementation strategies for each experiment category are presented as well as the respective test runs. The laboratory has been used to support courses in the curricula of the Bachelor of Science(B.Sc) in Computer, Electrical and Telecommunication Engineering Programmes at Makerere University.**

***Index Terms*—Counter, Shift Register, Clock, Interactive iLab Shared Architecture.**

I. INTRODUCTION

Ever since Makerere University adopted iLabs in 2005, several laboratories have been developed to support curricula of the BSc. in Computer, Electrical and Telecommunications Engineering Programmes [1]. The continuous research and development is intended to gradually fully integrate iLabs into curricula. Although past research has delved in fields where the dearth of hardware for the conventional laboratories was acute, present research lends more towards improving the functionality of the existing laboratories or addressing their inefficiencies. It is in this context that research toward developing the synchronous sequential logic iLab was undertaken.

In 2008, the iLabs@MAK Project undertook research leading to development of the combinational digital logic iLab. The laboratory, based on the NI ELVIS II hardware, hardware, supports experiments in areas of logic gate characterisation, combinational logic circuit synthesis and analysis. It is based on the batched mode of the iLabs shared Architecture (ISA) [2]. The main limitation of the iLab is the non-inclusion of a timing element, making it non complaint for handling synchronous sequential logic experiments. It's against this background that follow-up research was undertaken to develop an iLab which addresses the fields of memory elements, counters and shift registers.

Unlike combinational logic circuits that give instantaneous outputs dependent on only the inputs at that given time, sequential logic circuits have memory, with the outputs dependent on the inputs and stored data. In addition, the finite effect of the clock on the operation of the synchronous sequential logic circuits demands for real time monitoring of the experiment as it progresses. For these reasons, the interactive version of the ISA was chosen over the batched one. Unlike the batched architecture, the interactive iLab permits exclusive direct control of the experiment by the user for a specific time interval. The user can change the input parameters and observe the effects on the outputs as the experiment progresses.

The iLab interactive experiments architecture includes the interactive Service Broker, the Experiment Storage Service (ESS), Lab-side Scheduling Service (LSS), User-side Scheduling Service (USS) and the Lab Server. The ESS is a stand-alone web service that allows Service Brokers, Lab Servers and Lab Clients to store experiment data. The User-side Scheduling Service (USS) is used in conjunction with the Lab-Side Scheduling Service (LSS) to allocate lab time to users [3]. All these services are generic. In the latest version of the interactive ISA, the Lab Client is the front panel of the LabVIEW Virtual Instrument (VI) created for a particular lab. The Lab Server hence acts like a VI server, allowing users to access the user interface one at a time through a standard web browser. The remote users communicate with the hosted VI through the LabVIEW data socket transfer protocol. The various services available in the interactive architecture allow administrators to deploy the laboratory, and users to schedule access to the lab interface. The developer's role is to build suitable LabVIEW Virtual instrument (VI) to interact with and control a specific experiment setup on the hardware, and configure it for use within the interactive ISA.

II. CLOCK SIGNAL GENERATION ON THE NI ELVIS II+

A central aspect in the analysis of synchronous sequential logic circuits is that of the clock signal input. All synchronous sequential digital logic devices obtain their synchronism from a clock of some sort. The simplest clocks to generate in a laboratory are oscillators based on the charging and discharging of RC networks, as opposed to the crystal-controlled oscillators used in computers.

While using the NI ELVIS II+, several options are available for generation of a clock signal, viz: use of the Function Generator to produce a square wave, using the ELVIS DAQmx to generate a pulse train, which appears at the counter output terminal on the free scale board, and use of the 555 timer or any other Integrated Circuit in conjunction with other discrete circuit components in an astable circuit. Each of these methods has merits and demerits.

Internal clock generation on the NI ELVIS II+ can be done through creation of a pulse generation task in the Measurement and automation Explorer (MAX), and selecting either of the two counters for the physical channels; CTR0 or CTR1. This opens a configurable dialog box, in which the clock parameters are set.The sequential logic lab requires the clock to run continuously, so the generation is set to "continuos". When the task is run, the clock output appears on the counter output terminal, sat CTR0_OUT, and can be routed to the appropriate IC terminal, and one of the digital lines selected for reading, if it is required for visualise the clock plulses.

Within LabVIEW itself, the same task can be created using the DAQ assistantfollowing the same procedure. Fig.1 shows the resultant LabVIEW block diagram that results. It should be noted that continuous clock generation automatically requires a while loop within the VI. Since the ELVIS instruments required in the experiment setup, the digital reader and the digital writer also run continuously, it necessitates them to be in a while loop as well. The execution sequence in LabVIEW doesn't allow two parallel while loops to maintain synchronism, and this creates a time delay between the clock signal generated and the circuit it is intended to drive. It can thus be said that this method is suitable for clock generation and circuit control where the user does not mind loss of synchronism between the clock and the logical inputs/outputs.

Yet another method of generating a clock signal implemented using NI ELVIS II+ is the use of the Function Generator (FGEN) express VI within LabVIEW. To get a TTL compatible clock, the amplitude is set to 5V peak to peak voltage and the signal type is set to "square". On the bread board, the signal is picked from the FGEN terminal. From the FGEN output, this can be routed as an input to any IC terminal where the clock is required.Yet again, continuous clock generation requires a continuous run of the FGEN, necessitating a while loop around it. The catch situation is that the FGEN, the Digital Reader and the Digital Writer utilize the same DAQmx resources, and thus cannot be put in the same while loop. Thus, the FGEN, though availing a configurable clock source, was not suitable for the lab design, although it can be favorable in special instances with advanced VI design.

The best option for clock generation was by use of a 555 timer in the astable mode, because it could run without any resource conflicts and maintain perfect synchronism, albeit not providing flexibility regarding control of the clock parameters. Since the analysis of clock signal properties was a core component of the lab, use was made of the LabVIEW functionalities to create a simulated experiment which explores the properties of the clock generated by the 555 timer. This provides one of the experiments in the laboratory, as explained later.

III. LABORATORY DESIGN

Development of the synchronous sequential logic iLab involved both hardware and software design The hardware designs were accomplished using the integrated environment of NI Multisim, while the software designs were conceptualized in LabVIEW.For each of the experiment categories arising from the requirements specification, simulations were carried out in Multisim, utilizing the ELVIS bread board workspace and the simulated versions of the instruments. Where physical ICs were required, the simulated versions or close alternatives were used. From the working simulations, the physical hardware designs were derived. A typical case is illustrated in Fig.2, where the hardware design for the frequency division experiment is conceptualized. Design in Multisim achieves two ends: To begin with, most of the IC packages to be used in the physical circuit are presented in their simulated version, ensuring seamless transition from the simulation to the actual circuit. Secondly, the environment provides a workspace for the NI ELVIS breadboard for practice with the terminal configurations before working with the physical circuit. The simulation results also give an insight into the design of the suitable LabVIEW user interface to replicate or better the simulation controls. For example, since an oscilloscope provides timing diagrams in Multisim that are easy to analyze, the concept of creating the digital timing waveforms in the actual user interface came to mind at this level. Fig. 3 shows the typical output for the frequency division experiment as displayed on the Oscilloscope in Multisim.

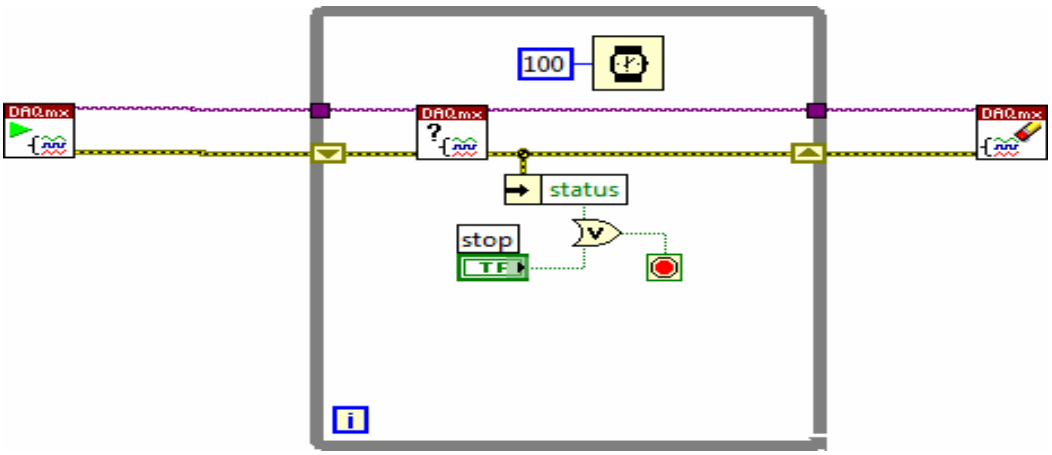

Figure 1. Low Level DAQmx Code for Clock Signal Generation in LabVIEW

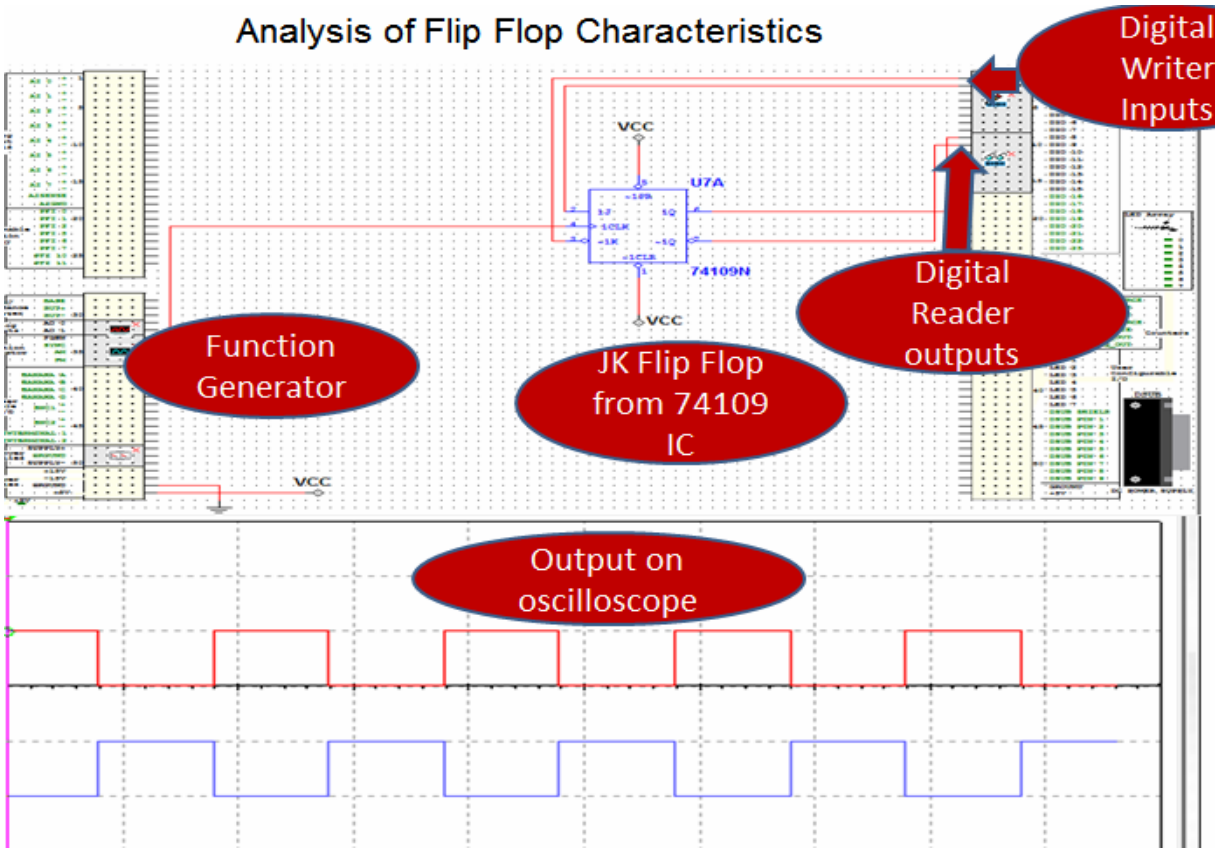

Figure 2. Experiment Hardware Design in Multisim

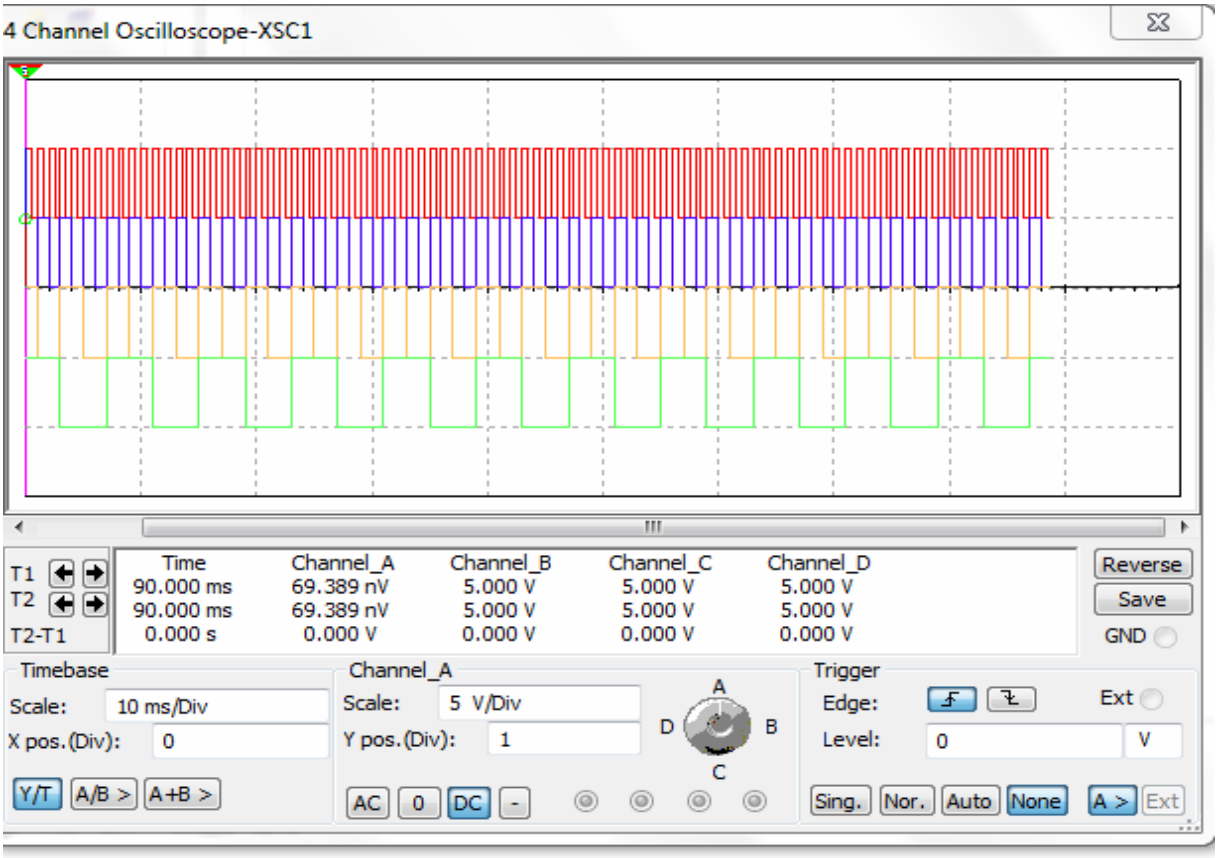

Figure 3. Frequency Division Simulation Results

IV. LABVIEW IMPLEMENTATION AND USER INTERFACE DESIGN

The ultimate stage in the implementation of the lab was done in LabVIEW. First, a conceptual framework of the user interface, whose model is shown in Fig.4, was developed. The user interface was designed to have inherent support for access multiple experiments during a single run.

The *Select Experiment* Option gives the lab user the option of running a specific experiment setup on the remote hardware while the rest are mute.

The *Instrument Configuration* enables users to set parameters for the relevant instrument controls. Emphasis has to be paid to the digital channels selected, since each experiment is tied to particular channels.

Run Experiment sends the command to start execution of the experiment on the remote hardware. Since the laboratory is interactive, the data is streamed in real time for analysis. This function was achieved by direct runs of the VI, with digital timing waveforms used for data presentation and analysis.

The Stop/Abort Execution call enables laboratory users to terminate the laboratory or switch between experiments. In case one user leaves the laboratory in progress, the next user is able to reset it.

To achieve access to multiple setups co-currently, a case structure was implemented; in which the requisite functions, inputs, controls and express VIs for the instruments were put.

The frequency division and counter experiments both utilize the same singular instrument, the digital reader but are put in different casesso as to have distinct timing behaviors on the front panel. As the clock runs, the U8 data, the numeric representation of the digital output digital output is converted into a Boolean array, then into an array of zeros and ones. Each of the output lines corresponds to a particular element in the array. Only the appropriate number of bits is indexed, corresponding to the lines being read, and then bundled to generate the stacked plots of the timing waveforms. The result is extensible, to cater for more output lines.

For the 555 timer a stable circuit, using various mathematical functions, formulae nodes and structures available in LabVIEW, a VI that allows users to change controls of all its circuit components and observe output signal as well as the respective output parameters was created.

The last case, created for the shift register experiment, utilizes both the digital reader and the digital writer, allowing a user to input a predefined binary sequence and analyze the output. Fig. 5 shows the lab user interface, incorporating all the different use cases.

With an appropriate VI created, the next step was integrating it into the interactive ISA version 3.0.4, setup on a desktop computer, and which would eventually provide the deployment environment for the laboratory. The procedures the interactive Lab Server with LabVIEW setup and configuration are well documented elsewhere, and so will not explained here. Since the interactive Lab Server setup utilizes the LabVIEW data socket transfer protocol, data sockets were attached onto all the input and output variables in the VI to facilitate remote control within a web browser, in which the client is rendered.

V. LABORATORY TEST RUNS

A typical deployment scenario for the frequency divider experiment is done using one 74S74 Dual D type flip flop, fixed on the ELVIS II+ breadboard, and biased with the static GROUND and +5V dc power supplies. The active low CLEAR and PRESET inputs are tied to +5V. The clock input is obtained from the 555 timer circuit. The setup has three input lines, DIO0, DIO1 and DIO2 corresponding to the clock frequency, and the frequencies at the outputs of each of the two cascaded flip flops. The user would thus select the DIO range 0-7 for the output data. There is no input data to manipulate in this case. An experiment would require a user to obtain the different frequencies, obtain the relationship between them, and possibly reverse engineer a digital circuit that would give that specific output. Fig.6 shows the typical run results of the experiment.

The platform created supports any form of counter experiment, setup either using discrete Flip Flops or specially made counter ICs. For the test run presented, the DM71LS161N synchronous 4 bit binary counter was used. The configurations of the IC can easily be obtained from its datasheet.The setup has four output lines, DIO8, DIO9, DIO10 and DIO11 corresponding to each of the four bits in the counting sequence. The user would thus select the DIO range 8-15 for the output data. The IC can be configured to achieve any counting pattern using other gates. The lab user would be required to derive the counting pattern from the output waveforms, derive a state transition diagram and postulate the possible connections at the remote end that achieve the output. Fig.7 shows typical results for the counter experiment.

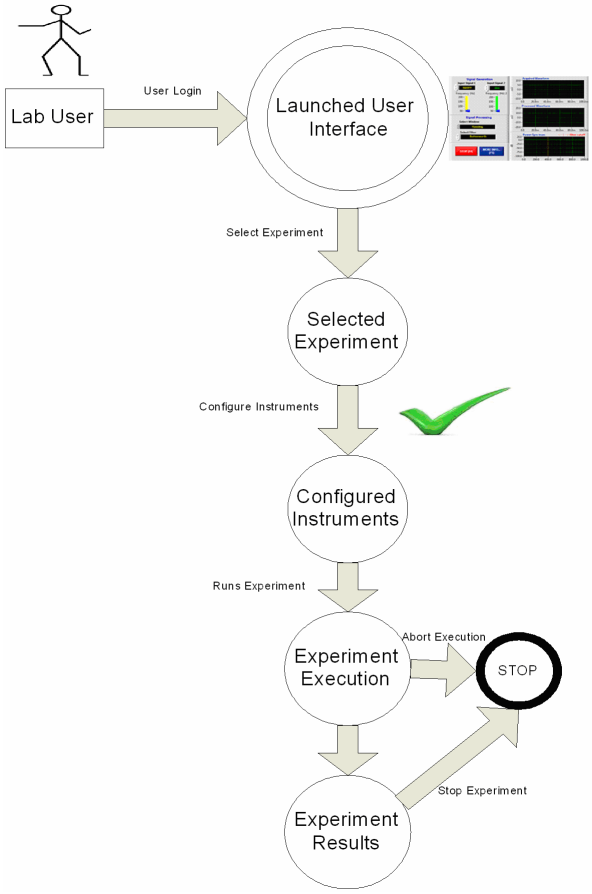

Figure 4. The User Interface Model

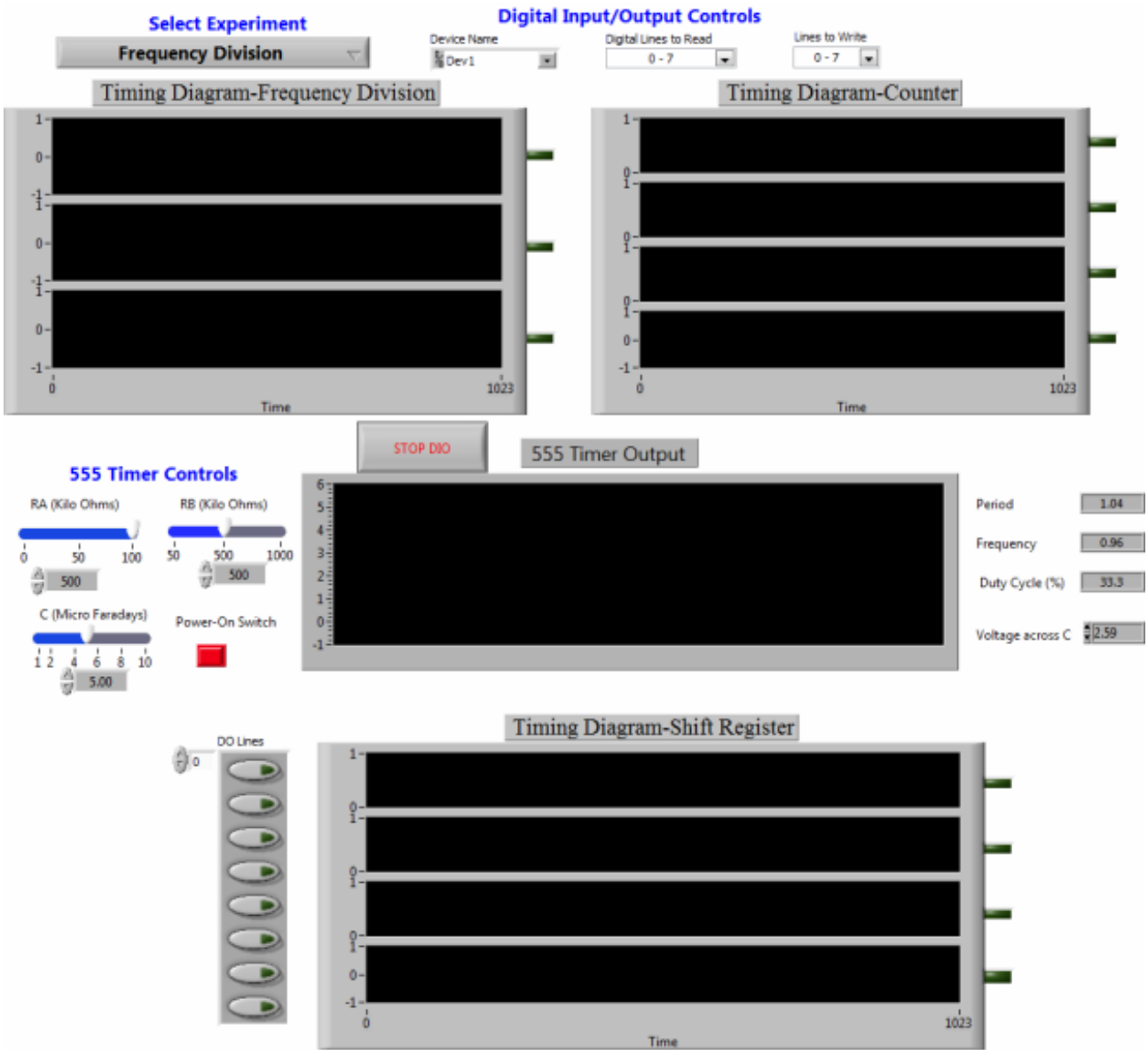

Figure 5. Sequential Logic User Interface

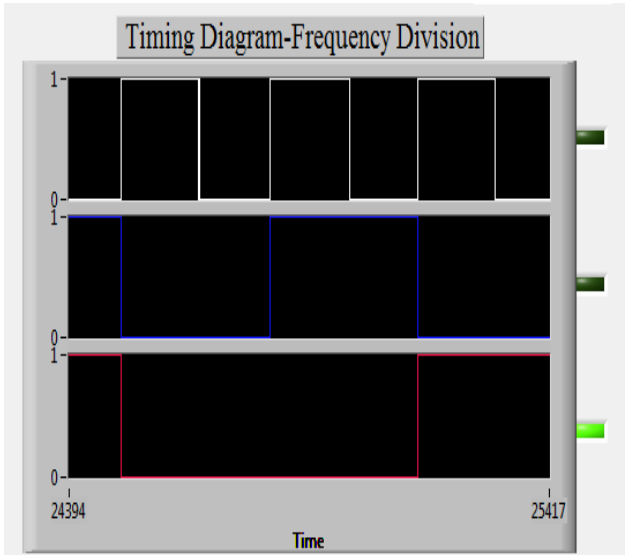

Figure 6. User Interface Results for Frequency Division

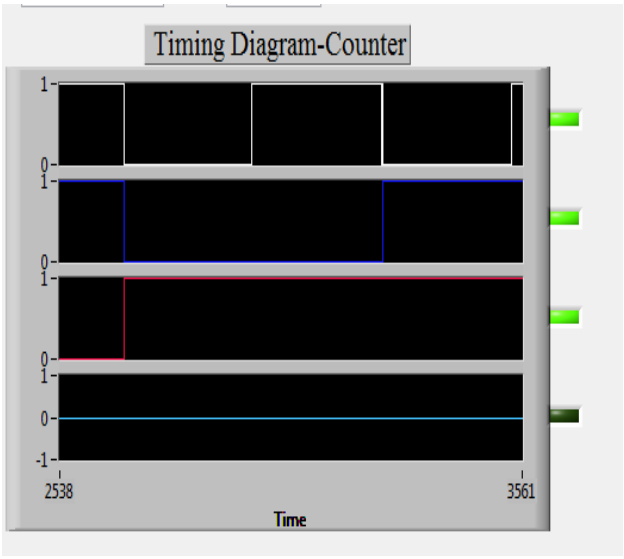

Figure 7. Counter Experiment Results

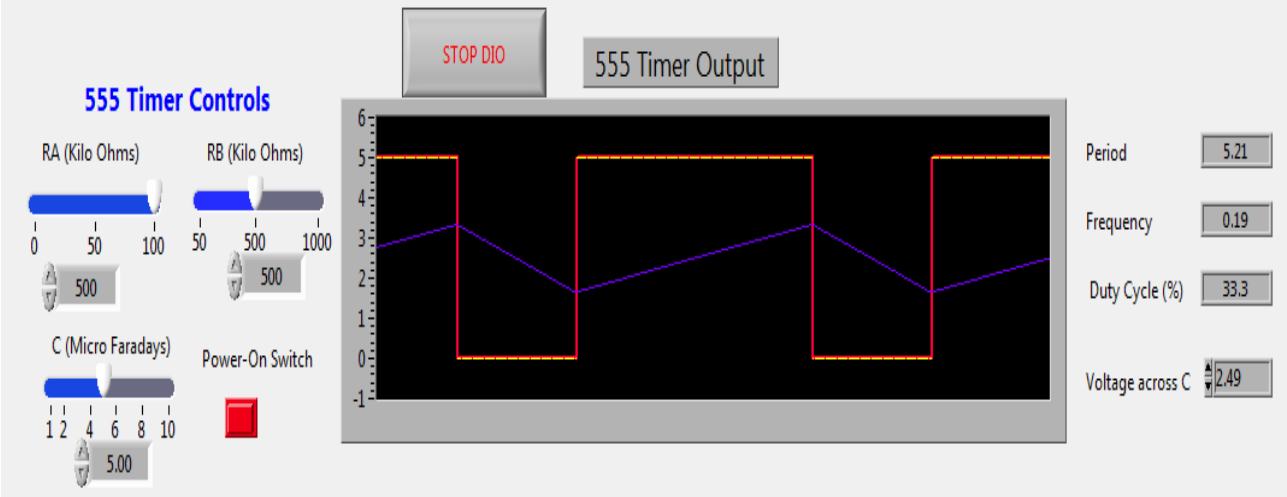

Figure 8. 555 Astable Circuit Analysis

The clock generation and analysis experiment involves configuring values for the 555 timer circuit input variables: R1, R2, and C, and observing the output clock signal. Although the developed user interface computes and displays the signal period, frequency and duty cycle, this feature can be disabled in an actual lab such that the lab users compute these values from the signal waveform, and compare with the theoretical values. Fig.8 shows typical results for this experiment.

Although the typical run scenarios presented in this section have given a glimpse into the capabilities of the laboratory, emphasis should be put on the generality of the platform since it can support experiments in each of the underlying categories, if the right components are setup.

VI. CONCLUSION

The development of the sequential logic iLab has contributed to increasing the number of online laboratories available at Makerere University. With the increasing student numbers coupled with dwindling laboratory hardware, the laboratory will play a huge role in improving the pedagogical experience of students and researchers at Makerere University, and globally.

The involvement of several stake holders during the course of the research: Makerere University, MIT, Busitema University, University of Dar es Salaam and National instruments in the requirements specification phase and implementation, is a silver bullet in a bid to foster collaboration in the development and utilization of iLabs. The iLabs@MAK Project has started the drive to extend iLabs to Busitema University, and this research plays to that tune.

Suffice to note is the fact that the iLab developed has limitations. It is important to have future research involving work on exposing the controls of the clock signal generated by the ELVIS so that users are able to flexibly apply it at different frequencies, and monitor the ensuing behaviour. As it is, the analysis is possible at a single frequency. The laboratory also does not support the input of binary streams; every digital line takes in one input at any given time. This makes it unsuitable for analysis of circuits such as serial-in registers. The user interface can also be improved by making it more interactive through inclusion of embedded instructions, tutorials, animations and any other content relevant to the lab.

It would also be beneficial to explore the possibility of integrating other logic boards into the laboratory, using the ELVIS II+ as the principal data acquisition device or by using the digital channels on any ordinary data acquisition card. This effort can extend the laboratory to incorporate real world data from physical systems other than restricting it to analysis of electronics components.

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This paper was made possible (in part) by a grant from Carnegie Corporation of New York under Grant No.BD3109.R04.The statements made and views expressed are solely the responsibility of the authors. It is an extended version of a paper resented at the Conference exp.at'11, held at Calouste Gulbenkain Foundation, Lisbon, Portugal, November 17-18, 2011. Received 17 May 2012. Published as resubmitted by the authors 21 July 2012.