

# A Novel Algorithm of Fundamental Positive Sequence Voltage Detector under Unbalanced and Distorted Voltages

<http://dx.doi.org/10.3991/ijoe.v9i3.2652>

Zhiqiang Wang, Jing Bian, Yawei Wang and Guofeng Li  
Dalian University of Technology, Dalian, China

**Abstract**—This paper presented a new algorithm for the performance improvement of fundamental positive sequence voltage extraction under unbalanced and distorted conditions. In this algorithm, an improved software phase-locked loop (SPLL) with a second order low-pass filter was proposed and analyzed, completely eliminating the phase detection errors of the unbalanced and distorted source voltages. The paper began with a description of the proposed fundamental positive sequence extraction method, and then a detailed analysis of the designed SPLL was introduced. The proposed algorithm improved the sinusoidal current control strategy of active power filter (APF) which was based on the classical power theories for obtaining an optimal extraction of the fundamental positive sequence current. To verify the feasibility of the algorithm in real-time applications, the simulation model was established in MATLAB-Simulink environment. Then, the algorithm was implemented in DSP using the TMS320F28335 development board. The results indicated that the proposed algorithm is feasible and effective, and it could be directly used in the practical applications.

**Index Terms**—Fundamental Positive Sequence Voltage Extraction, Software Phase-locked Loop, Low-pass Filter, Active Power Filter

## I. INTRODUCTION

Harmonic currents and reactive power generated by non-linear loads have a significant adverse impact on electrical distribution systems. The shunt active filter (APF) has been proved to be effective for the elimination of current harmonics and reactive power compensation. One of the cornerstones of APF is its control strategy for the real-time and accurate calculation of reference or compensating signal [1][2]. Many kinds of control strategies in a shunt active filter have been proposed so far, one of which is the Sinusoidal Source Current Control Strategy based on the  $pq$  Theory [3][4].

The sinusoidal source current control strategy is a principle of compensation that conducts the active filter to compensate the current of a non-linear load, and finally to achieve the result of making the compensated source current sinusoidal and balanced.

As the most important component in that strategy, the fundamental positive sequence voltage detector aims to improve the compensation performances under all voltage conditions, for example, voltage unbalances or voltage distortions.

For the extraction of fundamental positive sequence voltage, some literature has proposed detecting method based on the concept of space vector [4] or in frequency domain [5]. Reference [6] presented a performance comparison between a SPLL and an adaptive filter for detecting the fundamental positive sequence component. This paper proposes a much simpler algorithm just based on simple mathematics formula of trigonometric function which could be more useful in practice.

## II. ALGORITHM FOR FUNDAMENTAL POSITIVE SEQUENCE VOLTAGE DETECTOR

For a three-phase four-wire system, when the power system is unbalanced and distorted, the phase voltages contain positive sequence components, negative sequence components, zero sequence components and harmonic components.

Regarding the fundamental positive sequence detection, many extraction methods have been presented during the last years. The simple common methods are based on the detection of the peak value and zero crossing instants. Nevertheless, these methods might lead to significant angle and magnitude errors if facing unbalanced or distorted waveforms [7].

To solve this problem, we proposed a fundamental positive sequence voltage detector block, which uses a software phase-locked loop circuit locked to the fundamental frequency of the system voltages.

The overall principle block diagram of fundamental positive sequence voltage detector is shown as Fig. 1. It consists of coordinates transformation block, software phase-locked loop and low pass filter.

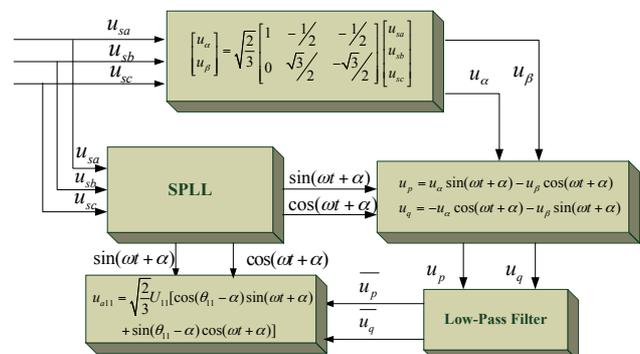


Figure 1. The principle block diagram of fundamental positive sequence voltage detector

Because the value of zero sequence components after  $dq$  transformation is zero, it needn't to be considered [8]. At this time, three-phase source voltages can be expressed as below.

$$\begin{cases} u_{sa} = \sqrt{2} \sum_{n=1}^{\infty} [U_{1n} \sin(n\omega t + \varphi_{1n}) + U_{2n} \sin(n\omega t + \varphi_{2n})] \\ u_{sb} = \sqrt{2} \sum_{n=1}^{\infty} \left[ U_{1n} \sin(n\omega t + \varphi_{1n} - \frac{2\pi}{3}) + U_{2n} \sin(n\omega t + \varphi_{2n} + \frac{2\pi}{3}) \right] \\ u_{sc} = \sqrt{2} \sum_{n=1}^{\infty} \left[ U_{1n} \sin(n\omega t + \varphi_{1n} + \frac{2\pi}{3}) + U_{2n} \sin(n\omega t + \varphi_{2n} - \frac{2\pi}{3}) \right] \end{cases} \quad (1)$$

Where  $U$  is the RMS value of source voltages,  $\omega$  and  $\varphi$  are the angular frequency and initial phase angle of source voltages; the subscript 1,2 donate the positive sequence component and the negative sequence component respectively; the subscript  $n$  donates the harmonic order (when  $n$  equals to 1, it donates the fundamental component). The three-phase voltages are transformed to  $\alpha\beta$  two-phase orthogonal coordinate by  $C_{32}$ , shown as below.

$$C_{32} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} u_{\alpha} \\ u_{\beta} \end{bmatrix} = \begin{bmatrix} \sqrt{3} \sum_{n=1}^{\infty} [U_{1n} \sin(n\omega t + \varphi_{1n}) + U_{2n} \sin(n\omega t + \varphi_{2n})] \\ \sqrt{3} \sum_{n=1}^{\infty} [-U_{1n} \cos(n\omega t + \varphi_{1n}) + U_{2n} \cos(n\omega t + \varphi_{2n})] \end{bmatrix} \quad (3)$$

In order to obtain the fundamental component, structure a transformation matrix  $C_T$  as below.

$$C_T = \begin{bmatrix} \sin(\omega t + \alpha) & -\cos(\omega t + \alpha) \\ -\cos(\omega t + \alpha) & -\sin(\omega t + \alpha) \end{bmatrix} \quad (4)$$

Where  $\omega t + \alpha$  is the phase angle of phase A getting from the SPLL.

Convert  $u_{\alpha}$  and  $u_{\beta}$  signals to  $u_p$  and  $u_q$  through  $C_T$ , shown as below.

$$\begin{bmatrix} u_p \\ u_q \end{bmatrix} = C_T \begin{bmatrix} u_{\alpha} \\ u_{\beta} \end{bmatrix} = \begin{bmatrix} \sqrt{3} \sum_{n=1}^{\infty} [U_{1n} \cos((n-1)\omega t + \varphi_{1n} - \alpha) - U_{2n} \cos((n+1)\omega t + \varphi_{2n} + \alpha)] \\ \sqrt{3} \sum_{n=1}^{\infty} [U_{1n} \sin((n-1)\omega t + \varphi_{1n} - \alpha) - U_{2n} \sin((n+1)\omega t + \varphi_{2n} + \alpha)] \end{bmatrix} \quad (5)$$

Equation (5) shows that the fundamental positive sequence component corresponds with DC value. Through a low pass filter, the other AC components in (5) could be eliminated and get the following result.

$$\begin{bmatrix} \overline{u_p} \\ \overline{u_q} \end{bmatrix} = \begin{bmatrix} \sqrt{3}U_{11} \cos(\varphi_{11} - \alpha) \\ \sqrt{3}U_{11} \sin(\varphi_{11} - \alpha) \end{bmatrix} \quad (6)$$

The fundamental positive sequence of phase A is given as.

$$\begin{aligned} u_{sa1} &= \sqrt{2}U_{11} \sin(\omega t + \varphi_{11}) \\ &= \sqrt{2}U_{11} \sin[(\omega t + \alpha) + (\varphi_{11} - \alpha)] \\ &= \sqrt{2}U_{11} \sin(\omega t + \alpha) \cos(\varphi_{11} - \alpha) + \sqrt{2}U_{11} \cos(\omega t + \alpha) \sin(\varphi_{11} - \alpha) \end{aligned} \quad (7)$$

That is,

$$u_{sa1} = \sqrt{\frac{2}{3}} \begin{bmatrix} \overline{u_p} \\ \overline{u_q} \end{bmatrix} \begin{bmatrix} \sin(\omega t + \alpha) & \cos(\omega t + \alpha) \end{bmatrix} \quad (8)$$

Where  $\sin(\omega t + \alpha)$  and  $\cos(\omega t + \alpha)$  are acquired from the software phase-locked-loop output and calculated by sine and cosine function. From (8), we know that the fundamental positive sequence of phase A could be extracted by a simple mathematical operation between (6) and sine and cosine value of the phase lock angle. Similarly, calculation formula of phase B and phase C are,

$$\begin{cases} u_{sb1} = \sqrt{\frac{2}{3}} \left\{ \overline{u_p} \left[ -\frac{1}{2} \sin(\omega t + \alpha) - \frac{\sqrt{3}}{2} \cos(\omega t + \alpha) \right] + \overline{u_q} \left[ -\frac{1}{2} \cos(\omega t + \alpha) + \frac{\sqrt{3}}{2} \sin(\omega t + \alpha) \right] \right\} \\ u_{sc1} = \sqrt{\frac{2}{3}} \left\{ \overline{u_p} \left[ -\frac{1}{2} \sin(\omega t + \alpha) + \frac{\sqrt{3}}{2} \cos(\omega t + \alpha) \right] + \overline{u_q} \left[ -\frac{1}{2} \cos(\omega t + \alpha) - \frac{\sqrt{3}}{2} \sin(\omega t + \alpha) \right] \right\} \end{cases} \quad (9)$$

### III. SPLL PRINCIPLE UNDER UNBALANCED AND DISTORTED VOLTAGES

#### A. Software Phase-locked Loop Working Principle

In grid connected converter applications, PLL is crucial for control algorithm performance [9]. The basic scheme of a classic PLL consists of a phase detector, a voltage controlled oscillator (VCO), a low-pass filter and a comparator [10]. Although the traditional PLL has been widely applied in electronic applications, it is not sufficiently immune to grid voltage variations.

Software implementation has several advantages including easy customization of the feedback loop that could timely change the multiplication or division ratio between the signal being tracked and the output oscillator. Hence, it may make sense to implement a phase locked loop in software for applications under unbalanced and distorted voltage conditions.

The proposed three-phase SPLL, operating in  $\alpha\beta$  and  $dq$  coordinates, is based on a second-order Butterworth low-pass filter. Compared to the classic algorithms, the proposed one is with a different structure, presented in Fig. 2.

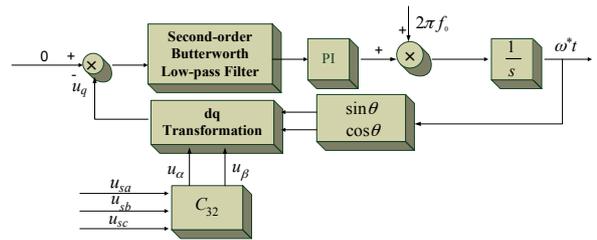


Figure 2. The principle block diagram of SPLL based on a second-order Butterworth low-pass filter

As shown in Fig. 2, for a three-phase software phase-locked loop, firstly convert voltage signals from  $abc$  axis to  $\alpha\beta$  axis through (2) and then  $\alpha\beta$  components are converted into  $dq$  rotating axis using (10).

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} \cos \omega^* t & \sin \omega^* t \\ -\sin \omega^* t & \cos \omega^* t \end{bmatrix} \begin{bmatrix} u_{\alpha} \\ u_{\beta} \end{bmatrix} \quad (10)$$

In the transformation matrix  $\omega^* t$  represents the SPLL output. The value of  $u_q$  reflects the phase difference between the input voltage and the output voltage of SPLL.

When  $u_q=0$ , it is supposed that phase-locked loop has tracked the input voltage phase angle. At this time,  $\omega^* t$  is the phase angle of input voltage.

But if the three-phase voltages are unbalanced and distorted,  $\omega^* t$  will include fundamental positive sequence phase, negative sequence phase and harmonic phase at the same time. In order to acquire the fundamental positive sequence voltage phase only, the value of  $u_q$  under unbalanced and distorted voltages (shown as (11)) is analyzed and get the conclusions as follows. After  $dq$  transformation, angular frequency of the positive sequence component decreases, and fundamental positive sequence component converts into DC value. While angular frequency of the negative sequence component increases, together with other harmonic components as AC value, the negative sequence component and harmonic components could be eliminated by a low-pass filter and get the phase angle  $\omega t + \alpha$  mentioned previously.

$$u_q = -\sqrt{3} \sum_{n=1}^{\infty} \{U_{1n}[\sin(n-1)\omega t + \varphi_{1n}] - U_{2n}[\sin(n+1)\omega t + \varphi_{2n}]\} \quad (11)$$

Literature [11] stated that SPLL system has a forward integral element, so it is inherently with the certain low pass filtering characteristic. However, when the voltages are distorted and unbalanced seriously, the AC amplitude of negative sequence component and harmonic components after  $dq$  transformation are so large that only relying on the filtering characteristic of SPLL can't fully filter all the AC components. So, an additional filter is introduced into the SPLL system. Taking both dynamic response and filtering effect of the filter into consideration, this paper chooses a second-order Butterworth filter.

#### B. Software Phase-locked Loop Performance Analysis

Fig. 3 shows SPLL system closed-loop transfer function diagram.

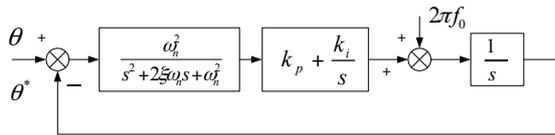


Figure 3. SPLL system closed-loop transfer function diagram

The PLL system closed-loop transfer function is

$$G_{close} = \frac{\omega_n^2 k_p s + \omega_n^2 k_i}{s^4 + 2\xi\omega_n s^3 + \omega_n^2 s^2 + \omega_n^2 k_p s + \omega_n^2 k_i} \quad (12)$$

Considering the impact that filter cutoff frequency makes on the system filtering effect, response speed, system stability and software realization degree, filter parameters are chosen as  $f_c=20\text{Hz}$  and  $\xi=0.707$ . Thus, equation (12) is written as

$$G_{close} = \frac{155753s + 3115060}{s^4 + 177.6s^3 + 15775.3s^2 + 155753s + 3115060} \quad (13)$$

According to the above parameters, bode diagram of the SPLL system is presented in Fig. 4.

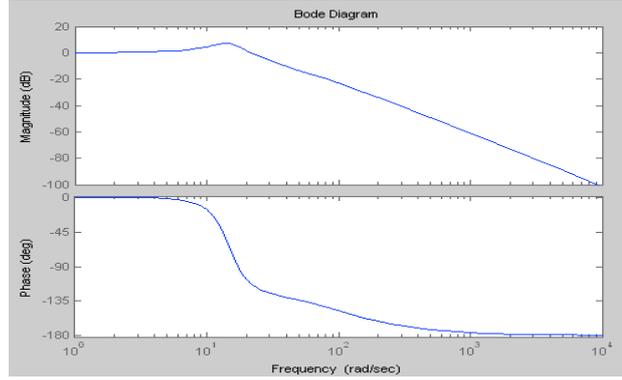


Figure 4. SPLL bode diagram (above is for magnitude, below is for phase)

The allowed frequency component in  $u_q$  is usually lower than 2 Hz therefore, the filter needs to eliminate other higher frequency components. As shown in the bode diagram, when  $f=50$  Hz, system gain is -30 dB and the phase is  $-157^\circ$ ; when  $f=100$  Hz, the gain is -53 dB and the phase is  $-174^\circ$ . These results indicate that this system has good filter characteristics.

#### IV. SYSTEM SIMULATION AND EXPERIMENTAL VALIDATION

##### A. Model Simulation Results

In order to validate the feasibility of the algorithm, a fundamental positive sequence voltage extractor Simulink model is built to simulate the three-phase voltages with harmonic components and asymmetric components. The extract result of phase A and phase lock result are respectively shown in Fig. 5 and Fig. 6, when source voltages are stacked with 20% five harmonic component and 12% fundamental negative sequence component to simulate distorted and unbalanced situation.

With the analysis of results, it is known that due to the existence of PI regulator and filter, during the first four cycles, phase-locked effect is not well established and frequency is below 50Hz. But only 0.08s later, phase-locked loop realizes the input signal's frequency tracking and phase tracking, and fundamental positive sequence extractor works accurately, extracting phase A fundamental positive sequence voltage signal in real-time.

Fig. 7 illustrates the extraction result when the harmonic and negative components disappear. System could still well track and extract corresponding fundamental voltage.

Through the above simulation, it is found that the extractor has fast response speed, good dynamic performance, which can complete the fundamental positive sequence voltage extraction timely and effectively under unbalanced and distorted voltages.

##### B. Software Validation based on TMS320F28335

TMS320F28335 is a floating-point digital signal processor. It adds a floating point arithmetic kernel to the DSP platform, making it easier to carry out complex floating point arithmetic and greatly save code execution time and storage space. It has much more merits such as high precision, large data and program memory space, together with more accurate A/D conversion, which are advantageous to be embedded in industry applications.

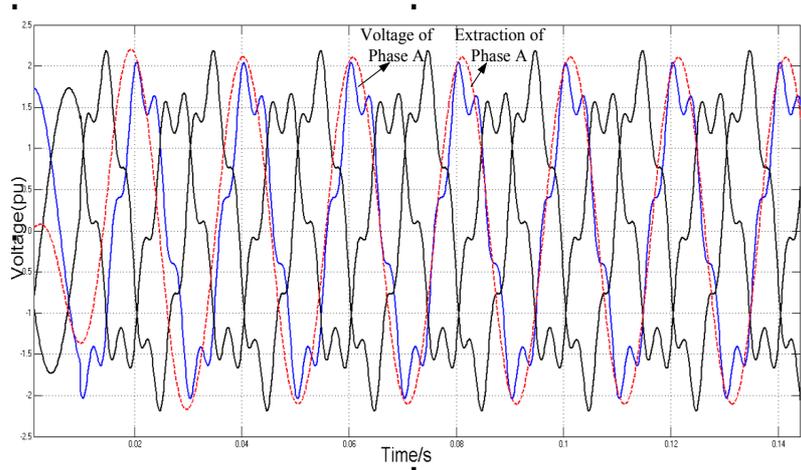


Figure 5. Fundamental positive sequence voltage extraction result of phase A under unbalanced and distorted voltages

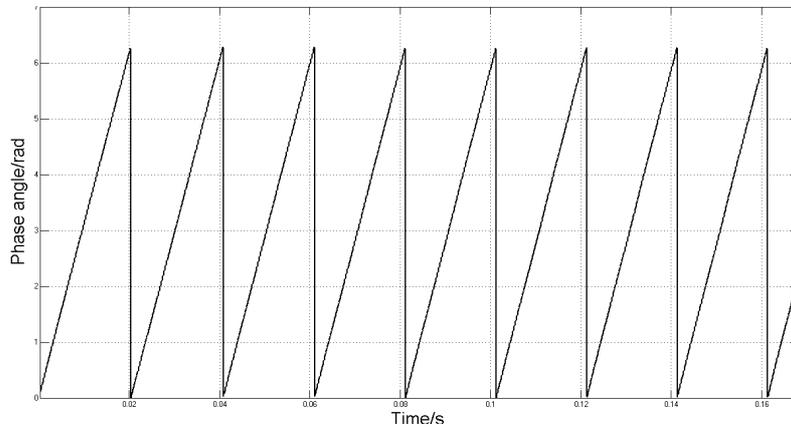


Figure 6. Phase lock result under unbalanced and distorted voltages

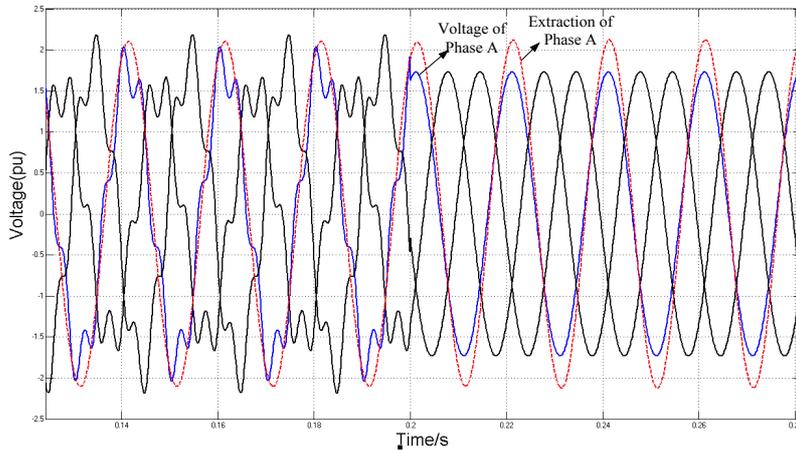


Figure 7. Fundamental positive sequence voltage extraction result of phase A when the harmonic and negative components disappear

This paper uses a TMS320F28335 DSP to verify the fundamental positive sequence voltage extractor principle. The characteristics of floating point arithmetic can quicken the speed of the algorithm. Sampling frequency is chosen as 10 kHz. Use the “graph-view” functions in CCS3.3 to observe the graph of input voltages and the extracted voltages.

Supposed the three-phase voltages are distorted and unbalance, for the convenience of observation, they are given as follows.

$$\begin{aligned}
 u_{a1} &= 311 \cdot \sin(\omega t - 12.6^\circ) + 120 \cdot \sin(5\omega t) \\
 u_{a2} &= 311 \cdot \sin(\omega t - 12.6^\circ - \frac{2}{3}\pi) + 10 \cdot \sin(\omega t - 12^\circ + \frac{2}{3}\pi) + 80 \cdot \sin(5\omega t - 12.6^\circ - \frac{2}{3}\pi) \\
 u_{a3} &= 311 \cdot \sin(\omega t - 12.6^\circ + \frac{2}{3}\pi) + 30 \cdot \sin(\omega t + 73.8^\circ - \frac{2}{3}\pi) + 14 \cdot \sin(5\omega t + 72^\circ + \frac{2}{3}\pi)
 \end{aligned} \quad (14)$$

Operation results are shown from Fig. 8 to Fig. 11.

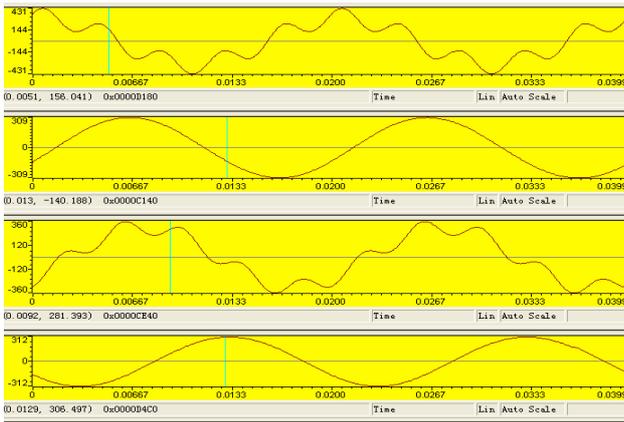


Figure 8. The waveform of input voltage and extracted fundamental positive sequence voltage at the first few cycles (from top to bottom respectively are phase A voltage waveform, extracted voltage of phase A, phase B voltage waveform and extracted voltage of phase B)

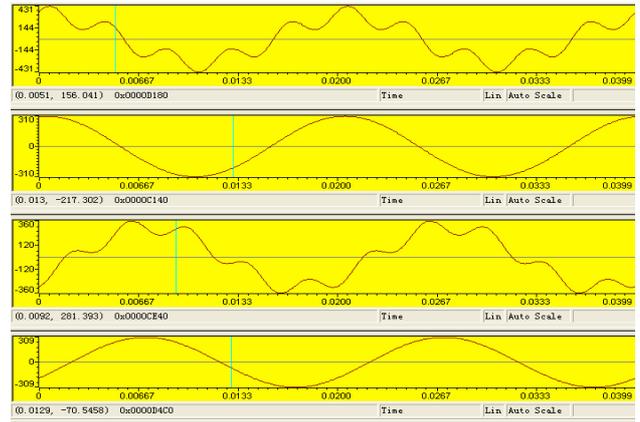


Figure 10. The waveform of input voltage and extracted fundamental positive sequence voltage when the system has achieved stability (from top to bottom respectively are phase A voltage waveform, extracted voltage of phase A, phase B voltage waveform and extracted voltage of phase B)

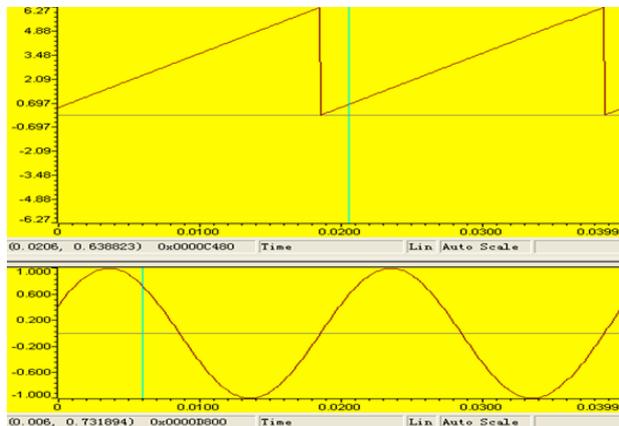


Figure 9. The waveform of SPLL output and its corresponding sine value during the first few cycles

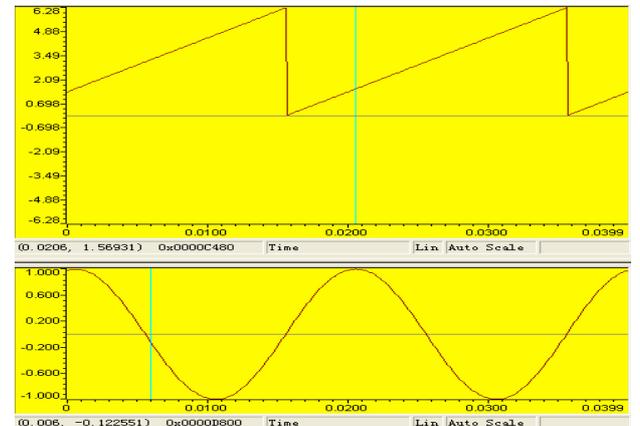


Figure 11. The waveform of SPLL output and its corresponding sine value when the system has achieved stability

As illustrated in Fig. 8 and Fig. 9, owing to the PI regulator and second-order filter in the SPLL, as well as the filtering link in the fundamental positive sequence extractor algorithm, there were some phase differences between output voltage and input voltage of extractor system during the first few cycles.

Although those processes cause a time delay, the fundamental positive sequence voltage detector still could get an accurate and excellent extract result just after about 4 cycles, as shown in Fig. 10 and Fig. 11. About 4 cycles, SPLL traces into the angle of phase A and realizes its fundamental positive sequence voltage amplitude and phase extraction. The output fundamental frequency is 50 Hz.

### V. CONCLUSION

Aimed at meeting requirements of fundamental positive sequence voltage in the sinusoidal current control strategy for APF, this paper introduces a new algorithm of fundamental positive sequence voltage extractor. The extractor algorithm contains a software phase-locked loop with an additional filter, strengthening the phase lock precision and voltage extraction accuracy. It can be used under unbalanced and distorted voltages, accurately extracting system fundamental positive sequence component with the corresponding amplitude and phase. In spite of the time delay, the response accuracy is guaranteed. In practical

applications, the system response speed can be adjusted according to actual requirements, and appropriate time compensation can be implemented to make the extractor algorithm further optimization.

### ACKNOWLEDGMENT

This work is partially supported by the Fundamental Research Funds for the Central Universities. The authors also gratefully acknowledge the helpful comments and suggestions of the reviewers, which have improved the presentation.

### REFERENCES

- [1] A. Chaoui, J. Gaubere and A.Bouafia, "Direct Power Control Concept and Analysis for Three Phase Shunt Active Power Filter", in *2012-38<sup>th</sup> Annual Conference on IEEE Industrial Electronics Society*, Montreal, 2012, pp. 1286-1294.
- [2] P. Acuna, L. Moran, M. Rivera, J. Rodriguez and J. Dixon, "Improved active power filter performance for distribution systems with renewable generation", in *2012-38<sup>th</sup> Annual Conference on IEEE Industrial Electronics Society*, Montreal, 2012, pp. 1344-1349.
- [3] H. Akagi, E. H. Watanabe and M. Aredes, *Instantaneous Power Theory and Applications to Power Conditioning*, John Wiley & Sons, 2007 <http://dx.doi.org/10.1002/0470118938>
- [4] H. R. Chen, Z. Xu, and F. Zhang, "Adaptive Detecting Method for Fundamental Positive Sequence, Negative Sequence Components

- and Harmonic Component Based on Space Vector”, In *Transmission and Distribution Conference and Exhibition, 2005/2006 IEEE PES*, Dallas, 2006, pp.726-732.
- [5] R.Langella and A. Testa, “A New Algorithm for Energy Measurement at Positive Sequence of Fundamental Power Frequency under Unbalanced Non-Sinusoidal Conditions”, In *Proceeding of the 2007 IEEE Lausanne Power Tech*, pp.1558-1563, 2007. <http://dx.doi.org/10.1109/PCT.2007.4538547>
- [6] H. Carneiro, B. Exposto and J. L. Afonso, “Evaluation of two fundamental Positive-Sequence Detectors for highly distorted and unbalanced systems”, In *11<sup>th</sup> International Conference on Electrical Power Quality and Utilisation, Lisbon*, 2011, pp. 1-6. <http://dx.doi.org/10.1109/EPQU.2011.6128883>
- [7] P. Rodriguez, R. Teodorescu, I. Candela, et al, “New Positive-sequence Voltage Detector for Grid Synchronization of Power Converters under Faulty Grid Conditions”, In *37th IEEE Power Electronics Specialists Conference*, 2006, pp.1-7. <http://dx.doi.org/10.1109/PESC.2006.1712059>
- [8] Y. X. Xie, K. P. Chen and Y. P. Deng, “Improved Detecting Method for Harmonic and Fundamental Active and Reactive Currents”, *Journal of South China University of Technology*, vol.33, no.4, pp.16-19, 2005.
- [9] B. Singh and S. R. Arya, “Software PLL based control algorithm for power quality improvement in distribution system”, In *2012 IEEE 5th India International Conference on Power Electronics*, Delhi, 2012, pp.1-6.
- [10] Z. X. Chen, Y. F. Li, L. G. Zhang, X. Y. Chen et al., “Based on fuzzy neural network of inverter power supply the controller design”, *International Journal of Digital Content Technology and its Applications*, vol.7, no.1, pp.379-385, 2013.
- [11] G. Zhou, X. C. Shi, C. Fu and Y. Wang, "Operation of a Three phase Soft Phase Locked Loop Under Distorted Voltage Conditions Using Intelligent PI Controller", in *Proceedings of the TENCON*, 2006, pp. 1-4.

## AUTHORS

**Zhiqiang Wang** is with School of Electrical Engineering, Dalian University of Technology, Dalian, China (e-mail: s200185004@mail.dlut.edu.cn).

**Jing Bian** is with School of Electrical Engineering, Dalian University of Technology, Dalian, China (e-mail: xinyisummer@yahoo.com.cn).

**Yawei Wang** is with School of Electrical Engineering, Dalian University of Technology, Dalian, China (e-mail: 549680229@qq.com).

**Guofeng Li** is with School of Electrical Engineering, Dalian University of Technology, Dalian, China (e-mail: guofenli@dlut.edu.cn).

This work was supported in part by the National High Technology Research and Development Program of China (863 Project) (No.2011AA060104). Received 05 April 2013. Published as resubmitted by the authors 21 June 2013.