A Broadband High Gain, Noise-Canceling Balun LNA with 3–5 GHz UWB Receivers for Medical Applications

Thaar A. Kareem[1,2(✉)], Hatem Trabelsi[1]
[1]National Engineers School of Sfax, University of Sfax, Sfax, Tunisia
[2]University of Misan, Misan, Iraq
`thaar_kareem@uomisan.edu.iq`

Abstract—The Ultra-Wideband Wireless Body Area Network (UWB-WBAN) has been identified to provide an efficient, low-power, and improved wireless communication between sensor nodes worn by the human body to monitor physiological signals. The first part of the UWB receiver is a low noise amplifier (LNA). This article describes an upgrade to a sort of balun LNA that is entirely transistor-based and devoid of inductors for medical worn communication service. The balun LNA uses common gate and a common source configuration which cancels the noise generated by the common gate. This work uses the transistors in place of resistors to minimize the integrated circuit's area, as well as finding the best values for the dimensions of the transistor to minimize energy consumption, achieve a high gain and good linearity. This reduces the noise figure. The designed system utilizes the UWB frequency range of 3–5 GHz and a voltage supply of 1.8V. The designed balun LNA is able to achieve a peak gain of 25.5 dB and noise figure (NF) less than 3.2–3.5 dB using 180μm TSMC CMOS technology. The IIP3 is quite high at 2 dBm, whereas the IIP2 maximum is 21 dBm. The entire power consumption is less than 7.2 mW.

Keywords—UWB, balun LNA, high gain, low NF, linearity, low power, CMOS

1 Introduction

A Wireless Body Area Network (WBAN) is a collection of sensors implanted or worn by the body. It allows information signals to be collected and communicated about a patient's health condition, such as heart rate and blood pressure, to a base station. This advancement aids in the prevention and diagnosis of issues while also preserving the patient's autonomy[1].

With the advancement in integrated circuits (IC) technology, biomedical applications with wireless communication have opened new paths to solve medical problems. The small-sized IC with low power consumption and transmission range can be embedded in the body and help in debugging the illness[2]. The modern circuits are inductorless to achieve the low cost and size[3]. The ultra wide band (UWB) technology is suitable for this. The UWB with a 7500 MHz bandwidth from 3.1 GHz to 10.6 GHz

[4][5] is approved by the Federal Communications Commission (FCC) in 2002. UWB has the advantages of low energy consumption and high transmission data rate. These advantages make the UWB a dominating technology [6]. UWB has grown in popularity due to its inexpensive cost, low transmission power, low power dissipation, high data rate, and resilience to multipath fading [7]. Due to hard attenuation of the transmitted signal, the signal at the received antenna is very weak. low noise amplifier (LNA) has to be used to amplify the received signal. The key objective of this article is to develop a very small, low-cost LNA with a high gain and good linearity LNA. Narrowband and wideband LNAs are readily available in the literature[8][9], but each has own drawbacks. Narrowband LNA makes the use of inductor circuits which make it bulky and energy hungry circuits. Though these have low noise figure but their integrated area is higher and requires technology with RF options to have inductors with high Q. On the other hand, wideband LNAs are complex in design. While RC wideband LNAs have a less complicated design, topologies exhibit high noise figures (NFs) [10]. Recently indcutorless LNAs are also proposed which unveils low NFs and require less on chip area [11][12].

The LNA design in this work is developed with the PMOS transistors as resistors [13]. As will be demonstrated, this strategy introduces a new degree of flexibility that may be exploited to optimize the LNA gain and, therefore, the circuit NF.

This document is structured in the following manner. In Section 2 and 3, we do an AC analysis to extract the equations for the balun LNA's basic CG and CS stages. We offer simulation findings for the typical LNA in Section 4. In Section 5, we compare the performance of this LNA to that of others previously published. Finally, Section 6 concludes the paper.

2   Balun LNA analysis

A critical option must be taken while designing a wideband LNA. A single-ended LNA doesn't need a balun to convert the single input to differential as balun reduces the NF substantially and higher losses[11]. It needs only the antenna and RF filters. However, the differential input gives lesser harmonic distortions and improved power supply with noise rejection.

The advantages of both single-ended and balun are used to investigate the LNA (see Figure 1) to design the simple and low-cost LNA. The load resistors have been eliminated in this design in favor of PMOS transistors and (M_3, M_4) that operate in the triode region and are ideally approximated by a resistor between the drain and source.

$$r_{ds} = \frac{1}{g_{ds}} \tag{1}$$

Where g_{ds} is the channel conductance. To compare the suggested design with the LNA with load resistors, the initial design specifies the same resistance value for r_{ds} as in the LNA with load resistors.
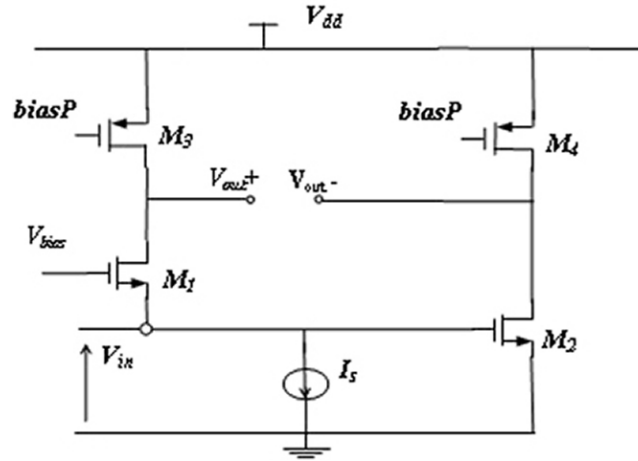
Fig. 1. Balun LNA

The suggested inductorless balun LNA circuit with combined common gate (CG) and common source (CS) configuration is illustrated in Figure 1. The single-ended input signal is amplified and transformed into differential output. The CG M1 transconductance g_{m1} governs the input impedance of this circuit. The noise at the input transistor M_1 is canceled when the gain of CS and CG are equal and opposite [14][15]. Additionally, distortion cancellation is possible, enabling the development of very linear LNAs. The impedance matching at the input is achievable if the CG-stage Z_{inCG} input impedance equals to the source resistance R_s. We can modify the current in M_2 by adjusting the DC voltage (Vbias) at the gate of M_1 in order to get an equal voltage gain at Vout+ and Vout–. The DC voltage (biasP) is utilized to alter the magnitude and NF of the LNA by adjusting the output conductance g_{ds3} and g_{ds4} of M_3 and M_4, respectively.

3 Small signal analysis

Figures 2 and 3 represent equivalent small signal circuits of the common-gate stage and common-source stage, respectively. In the following equation g_m and g_{mb} are the transistor's transconductance and body effect transconductance, respectively, r_o is the transistor's output resistance. The capacitance C_{gs} gate-source capacitance. C_{gd} gate-drain capacitance, C_{sb} source-bulk capacitance and C_{db} drain-bulk capacitance. R_s is the signal source resistance. We denote by A_{CG} and A_{CS} the voltage gain of common-gate circuit and common-source circuit, respectively.
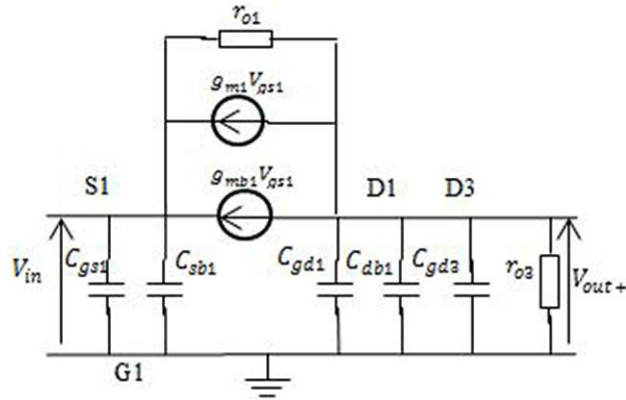
Fig. 2. Small signal circuits of the common-gate stage

3.1 Small signal equivalent circuit common-gate and common-source stage

In Figure 2 we denote by $Z_1 = r_{o3} \parallel \dfrac{1}{jC_{13}w}$ and $C_{13} = C_{gd1} + C_{db1} + C_{gd3}$. Here $V_{in} = -V_{gs1}$; when summing the currents on the output result in:

$$\frac{V_{out}^{+} - V_{in}}{r_{o1}} - g_{m1}V_{in} + \frac{V_{out}^{+}}{Z_1} = 0 \tag{2}$$

Now solving for $\dfrac{V_{out}^{+}}{V_{in}}$

$$A_{CG} = \frac{V_{out}^{+}}{V_{in}} = \frac{r_{o3}\left(1 + \left(g_{m1} + g_{mb1}\right)r_{o1}\right)}{r_{o3} + r_{o1} + jwC_{13}r_{o1}r_{o3}} \tag{3}$$
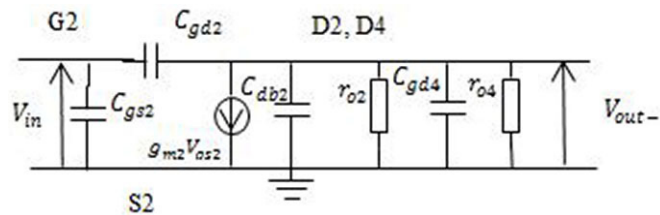

Fig. 3. Small signal circuits of the common-source stage

3.2 Small signal equivalent circuit common-source stage

For the common-source stage Figure 3 we denote by $R_o = r_{o2} \parallel r_{o3}$ and $C_{24} = C_{db2} + C_{gd4}$

Here $V_{in} = V_{gs2}$; summing the currents on the output result in:

$$\left(V_{out}^- - V_{in}\right) jwC_{gd4} + g_{m2}V_{in} + \frac{V_{out}^-}{R_o \parallel \frac{1}{jw(C_{24})}} = 0 \tag{4}$$

Solving for $\frac{V_{out}^-}{V_{in}}$ gives the voltage gain of common-source circuit:

$$A_{CS} = \frac{V_{out}^-}{V_{in}} = -g_{m2}R_o \tag{5}$$

Capacitors C_{gs3} and C_{gs4} of transistors M_3 and M_4 don't affect the frequency behavior because both sides are connected to the AC ground. The differential gain of the LNA is given by:

$$G = \frac{\left(V_{out}^+ - V_{out}^-\right)}{V_{in}} = A_{CG} - A_{CS} \tag{6}$$

If we neglect the effect of parasitic capacitance and g_{mb}, the common-gate voltage gain will be:

$$A_{CG} = \frac{V_{out}^+}{V_{in}} = \frac{r_{o3}\left(1 + g_{m1}r_{o1}\right)}{r_{o3} + r_{o1}} \tag{7}$$

and the common-source voltage gain will be:

$$A_{CS} = \frac{V_{out}^-}{V_{in}} = -g_{m2}R_o = -g_{m2}\frac{r_{o2}r_{o4}}{r_{o2} + r_{o4}} \tag{8}$$

In order to have a differential output circuit and cancels the output noise, the magnitude of the two gains should be equal. This is possible if we make; $r_{o3} = r_{o4} = r_{oPmos}$; $r_{o1} = r_{o2} = r_{oNmos}$; $(g_{m1} + g_{mb1})r_{o1} \gg 1$ and neglecting the transistor body effect. Then $g_{m1} = g_{m2}$, so, it's important to fix the same length dimension $L_1 = L_2 = 0.18\mu m$ of the transistors M1 and M2. If we take in account those conditions the LNA gain will be expressed as in (9):

$$A_{LNA} = \frac{\left(V_{out}^+ - V_{out}^-\right)}{V_{in}} = A_{CG} - A_{CS} = 2g_{m1}\frac{r_{oNmos}r_{oPmos}}{r_{oNmos} + r_{oPmos}} \tag{9}$$

Indeed to attain the best performance a suitable scaling of the CS stage is required not only for a lower noise figure but also for lower distortion too. The nonlinearity of the transconductance g_m and the output conductance g_{ds} are the principal cause of this distortion besides the dependence of g_m on the drain source bias voltage [14]. More a best balun –LNA linearity is obtained if the CS stage has the best linearity.

As the input impedance of the LNA is very significant for the overall receiver performance

$$Z_{inLNA} = Z_{inCG} \tag{10}$$

$$I_{inCG} = V_{in}jw(C_{gs1} + C_{sb1}) - \frac{V_{out}^+ - V_{in}}{r_{o1}} - \left(g_{m1} + g_{mb1}\right) * V_{gs1} \tag{11}$$

We denote $C_2 = C_{gs1} + C_{sb1}$ and $C_3 = C_{gd1} + C_{db1} + C_{gd3}$

$$-\frac{V_{out}^+ - V_{in}}{r_{o1}} - (g_{m1} + g_{mb1}) * V_{gs1} = \frac{V_{out}^+}{r_{o3}} + V_{out}^+ * jwC_3 \tag{12}$$

$$V_{out}^+ = \left[\frac{r_{o1+}r_{o3}}{r_{o1}r_{o3}} + jwC_3\right] = \left(g_{m1} + g_{mb1} + \frac{1}{r_{o1}}\right)V_{in} \tag{13}$$

$$V_{out}^+ = \frac{g_{m1} + g_{mb1} + \dfrac{1}{r_{o1}}}{\dfrac{r_{o1+}r_{o3}}{r_{o1}r_{o3}} + jwC_3}V_{in} \tag{14}$$

$$I_{inCG} = jwC_2 V_{in} - \frac{g_{m1} + g_{mb1} + \dfrac{1}{r_{o1}}}{\dfrac{r_{o1+}r_{o3}}{r_{o1}r_{o3}} + jwC_3}V_{in} + \frac{1}{r_{o1}}V_{in} + (g_{m1} + g_{mb1})V_{in} \tag{15}$$

$$\frac{I_{inCG}}{V_{in}} = jwC_2 - \frac{g_{m1} + g_{mb1} + \dfrac{1}{r_{o1}}}{\dfrac{r_{o1+}r_{o3}}{r_{o1}r_{o3}} + jwC_3} + \frac{1}{r_{o1}} + (g_{m1} + g_{mb1}) \tag{16}$$

$$\frac{1}{Z_{inCG}} = jwC_2 - \frac{g_{m1} + g_{mb1} + \dfrac{1}{r_{o1}}}{\dfrac{r_{o1+}r_{o3}}{r_{o1}r_{o3}} + jwC_3} + \frac{1}{r_{o1}} + (g_{m1} + g_{mb1}) \tag{17}$$

Neglecting the capacitance effects, we obtain

$$\frac{1}{Z_{inCG}} = -\frac{g_{m1} + g_{mb1} + \dfrac{1}{r_{o1}}}{\dfrac{r_{o1+}r_{o3}}{r_{o1}r_{o3}}} + \frac{1}{r_{o1}} + (g_{m1} + g_{mb1}) \tag{18}$$

$$Z_{inCG} = \frac{r_{o1+}r_{o3}}{r_{o1}(g_{m1} + g_{mb1}) + 1} \tag{19}$$

4   Simulation and result

The analysis and simulation of the proposed wideband LNA is evaluated on the gain, noise figure and linearity. The simulation is done with the help of Advanced Design System (ADS) tool and TSMC RF 0.18 μm CMOS process.

4.1 Gain, S11 and NF

The S_{11} plot in Figure 4 shows that the S_{11} is less than −15 dB for the frequency range of 3–5 GHz, which indicates that the designed LNA has good reflected coefficients in this frequency band. The range of the gain is equal 25.5–22.47 for the frequencies 3 to 5 GHz which means we have a good performance for the gain, shown in Figure 5. The wideband LNA consumes 7.2 mW at a Vdd of 1.8 V.
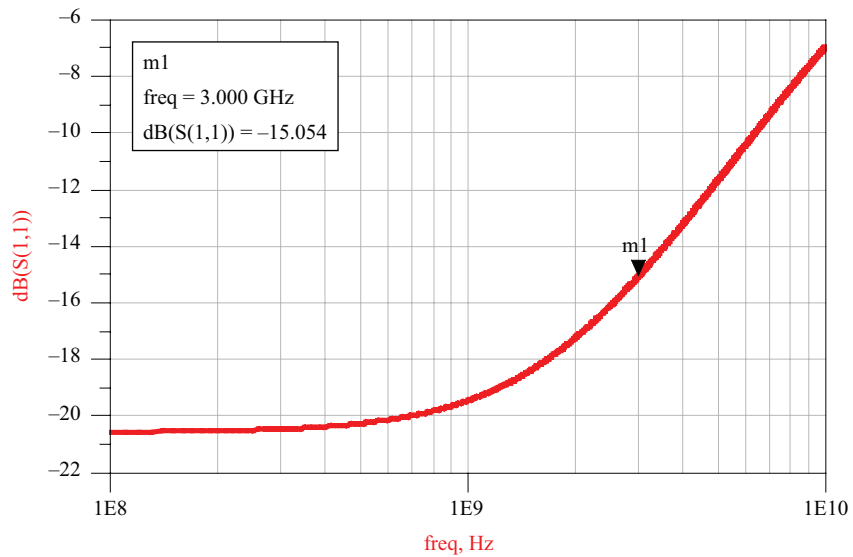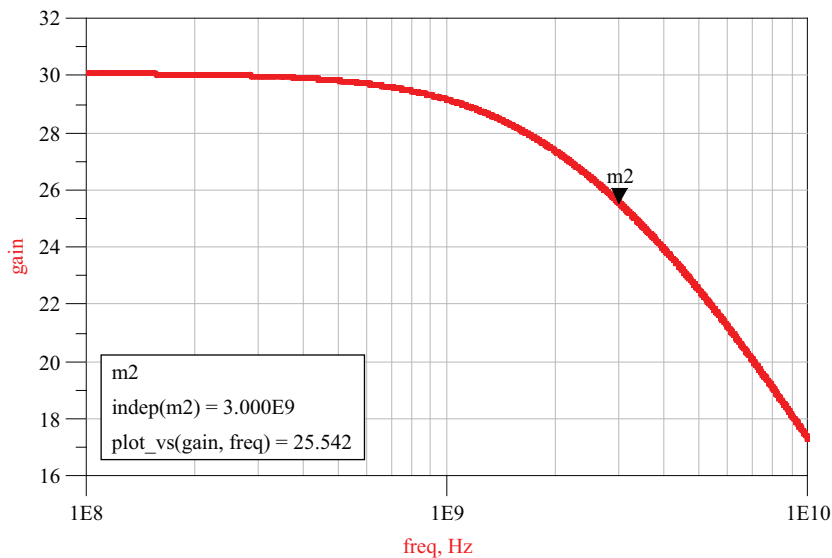

Fig. 4. S11 of the LNA

Fig. 5. Gain in dB of the LNA

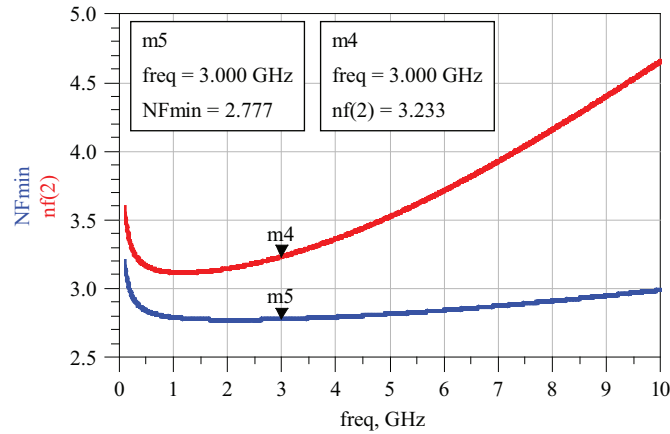As shown in Figure 6, the Noise figure (NF) vary from (3.2 dB to 3.5 dB) for the frequencies 3 to 5 GHz.

Fig. 6. NF of the LNA

4.2 Linearity, IIP3, IIP2 and P-1dB

The distortion performance is analyzed in the simulation for the second and third intermodulation intercept input IIP2 and IIP3, respectively and is depicted in Figures 7 and 8. An IIP3 of 2 dBm and IIP2 = 21.018 dBm are achieved and a 1 dB compression point P-1dB(in dBm) = –14 dBm as shown in Figure 9. Knowing that the UWB receiver receives a maximum power of –41.3 dBm/Mhz, the values found by simulation show that the LNA has an excellent linearity performance.
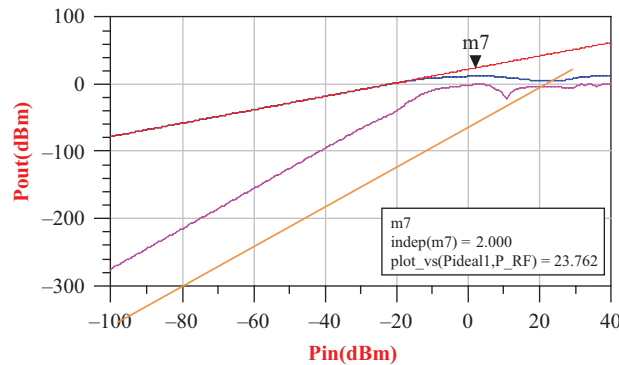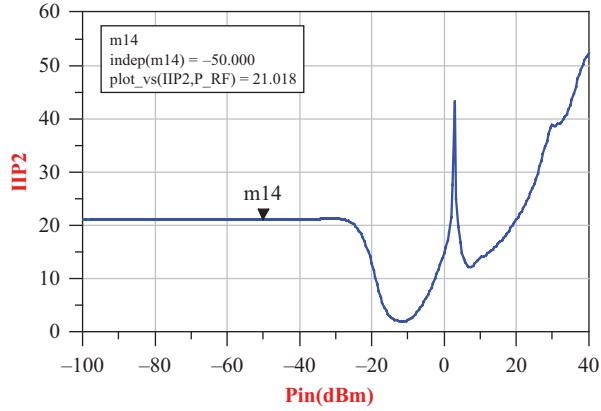

Fig. 7. IIP3 of the LNA

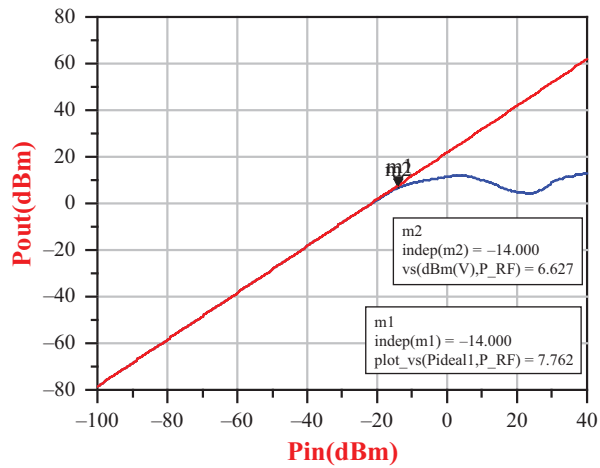**Fig. 8.** IIP2 of the LNA

Fig. 9. P-1dB(in dBm) of the LNA

5 Comparison

The results of the proposed circuit are compared with the state-of-the-art works, which devoid the inductor usage and are shown in Table 1. That the balun usage at the input with a mix of common source and common gate configuration has increased the gain, minimized the NF, reduces the IIP3 and improves the linearity.

Table 1. LNA comparsion

	Freq. band (GH)	Tech. (nm)	Gain (dB)	NF (dB)	IIP2 (dBm)	IIP3 (dBm)	Power (mW)	S11
[6]	3–5	180	17	8–9	–	–	26.6	<–10
[7]	0.2–10	130	12.2	3.2	6.2	0.7	4.8	<–10
[16]	3–5	180	16.8	2.6–3.1		–3.47	35.1	<10
[17]	0.2–5.2	65	13–15	<3.5	>+20	>0	21	<–10
[18]	0.8–6	90	18–20	<3.5	–	>–3.5	12.5	<–10
This work	3–5	180	25.5–22.4	3.2–3.5	21.02	2	7.2	<–15

6   Conclusion

This article proposed a wideband LNA structure for high gain and low noise figure with excellent linearity performance. The proposed circuit can amplify the signals of frequencies between 3 GHz and 5 GHz with a gain ranging from 25.5 dB to 22 dB respectively, which shows good wideband performance. The design is based on the MOSFET only and uses the balun to convert the single-ended input to differential output with a mix of common gate and source stages. The analytical solution is also derived for gain and input matching. The validation of analytical solution is done through simulation in ADS software. The 180 nm CMOS technology simulation shows that, the NF is 3.2 to 3.5 dB for a power consumption of 7.2 mW. The inductorless Balun-LNA is optimized in order to provide minimal NF, very good linearity, good gain, small chip area and low cost while consuming low power. This obeys to mostly chip constrains. In conclusion, the proposed inductorless Balun-LNA is the best candidate for the UWB transceiver used in the WBAN nodes.

7   References

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8 Authors

Thaar A. Kareem is a lecturer in Electric Engineering Department—College of Engineering, University of Misan, Iraq. He obtained BSC from university of Baghdad, Iraq and the master from EMU, north Cyprus. Now he is a PhD student in Systems Integration & Emerging Energies Laboratory, Electrical Engineering Department, National Engineers School of Sfax, University of Sfax B.P. 1173, Sfax 3038, Tunisia, E-mail: thaar_kareem@uomisan.edu.iq.

Hatem Trabelsi was born in Sfax, Tunisia in 1969. He received the engineering degree in electrical engineering from the National School of Engineers of Tunis in 1993, the aggregation degree in 2001, Ph.D. in electrical engineering in 2009 and HDR in electrical engineering from the National School of Engineers of Sfax in 2015. His research was mainly focused on Microelectronic circuit design and implementation of ultra low power transceivers for Wireless Sensor Network. He is a member of the research laboratory Systems Integration & Emerging Energies Laboratory (SI2E), ENIS, where he is working in the field of analog and RF circuit design for ultra-wideband systems. His research interests are single-chip CMOS transceivers, RF front-ends, Ultra wideband analog circuit design. He is the author and co-author of several papers in the Microelectronic field. He is currently a Professor at the Electrical Engineering Department of the National School of Engineers of Sfax, University of Sfax B.P. 1173, Sfax 3038, Tunisia, E-mail: hatem.trabelsi@enis.tn.