

Analysis of the Deadbeat Control Algorithm for Photovoltaic Grid Connected Inverter Output Current

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Abstract—Photovoltaic grid connected inverter is the core interface device in the photovoltaic power generation system to grid. The power quality of photovoltaic power generation system is affect by the waveform of output sinusoidal AC current directly. In this paper, current deadbeat control algorithm and a two-stage photovoltaic grid-connected inverter control strategy are proposed by analyzing the derivation of a photovoltaic grid-connected inverter. According to the grid connected Photovoltaic system features, a set of three-phase Photovoltaic grid connected inverter is designed, which rated power is 15 kW. The deadbeat control algorithm is introduced, based on the analysis of photovoltaic grid connected inverter topology, grid connected voltage, current, power, and the current waveform distortion rate. The deadbeat control algorithm is effective to control the three phase inverter output current through the system simulation and analysis.

Index Terms—grid connected inverter, topology, deadbeat control, system simulation.

I. INTRODUCTION

With the problems of energy shortage and environmental pollution growing, the development of clean and renewable energy is more and more concerned in the world [1-5]. Photovoltaic power generation technology have continued development, which has become one of the main ways of utilizing solar energy in latest 20 years.

Grid connected inverter is the most important interface equipment for photovoltaic power systems and grid. The goal of system control is to achieve sinusoidal AC output, because of the output current waveform of the power quality directly affect the photovoltaic power generation systems. So the grid inverter output current control strategy to become one emphasis of the photovoltaic power generation system research [6]. There are several methods that applied in inverter output current control, such as deadbeat control algorithm, PI control, spatial vector control method (SVPWM), stagnant loop control method etc [7]. As detailed in [8], the existing full-bridge-type and half-bridge-type converters have been analyzed by using the developed model and rules, and a new full-bridge-type converter structure and a compensation strategy for half-bridge-type inverter have been presented. As detailed in [9-15], some of the topologies are pointed out as the best candidates for either single PV module or multiple PV module applications.

In this paper, the deadbeat control algorithm is adopted to control the output current of 15KW photovoltaic inverter system through the analysis.

II. CONTROL OF GRID-CONNECTED INVERTER

PV grid-connected inverter block diagram is shown in Fig. 1. The MPPT part is DC voltage and AC current cycle. The Boost circuit with three-phase inverter circuit can be independently controlled by two controllers, and PV array with multiple boost circuit of the high DC voltage output [16-18]. The MPPT with DC voltage and grid current cycle are independent, because of the Boost circuit output voltage of the solar is increased. Boost circuit according to the characteristic of the solar cell, adjusting the duty cycle to regulate the working voltage of the solar cell, thus ensuring the photovoltaic array operating at maximum power point [19-22]. Boost circuit output voltage of the solar cell is increased.

The Maximum Power Point Tracking control block is shown in Fig. 2. The control scheme provides an optimized simple and effective maximum power point tracking control algorithm (Maximum Power Point Tracking, MPPT) of the PV array maximum power output under different light and temperature conditions change. The cost of system indirect was reduced, when improving the conversion efficiency of the PV array. Synchronous rotating coordinate system, the application of an electric current vector PI control method, which both to achieve synchronization with the mains voltage of the inverter output current (power factor is one) and grid current closed-loop control. The current impact to the grid can be solving to photovoltaic power generation control system.

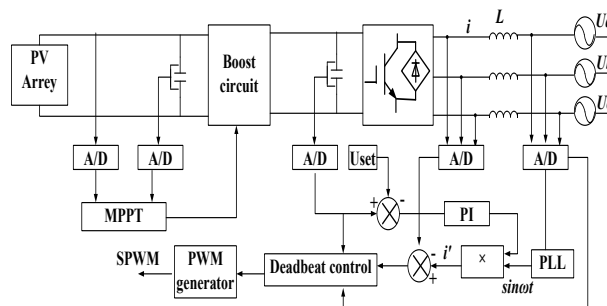


Figure 1. Structure of the inverter based on deadbeat control

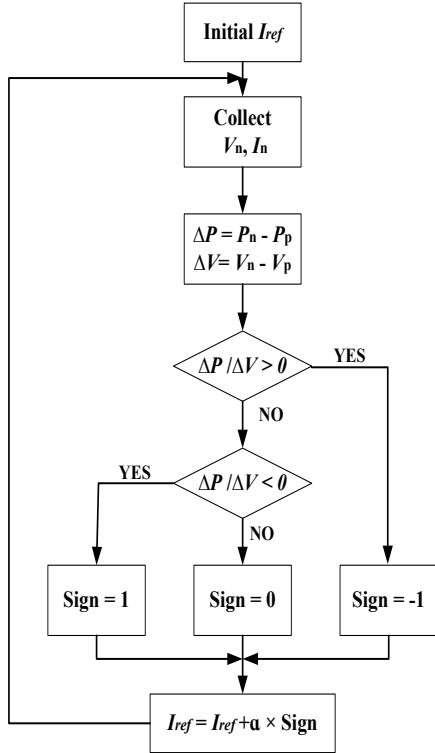


Figure 2. The control block diagram

III. TOPOLOGY OF GRID CONNECTED INVERTER

Grid connected inverter is core device of photovoltaic power. The function of the inverter is photovoltaic cells DC power can be converted into AC power, and transmitted to the grid.

The topology of Single-stage photovoltaic grid connected inverter is shown in Fig.3.

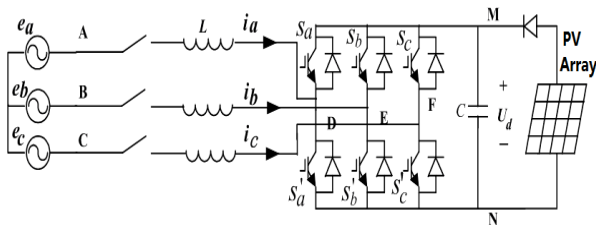


Figure 3. Topology of grid connected inverter system

Where e_a, e_b and e_c are the three phase power supply voltage, i_a, i_b and i_c are the three phase current of grid connected inverter, L is the reactor inductance, C is the capacity of DC side, U_d is the voltage capacitor, $S_a, S_b, S_c, S_a', S_b', S_c'$ are the device of insulated gate transistor (IGBT).

IV. DEADBEAT CONTROL ALGORITHM

The main objective of the proposed control is to achieve low harmonic distortion in the grid current even during grid abnormal conditions. Deadbeat control algorithm is a control algorithm depends on the circuit parameters used in the inverter system modulation algorithm will lead to inconsistent. When the cycle of control is beginning, a voltage vector, that the error tends to zero, is selection to control the inverter switching device.

The voltage equations of the loops ADNEB, BENFC, and CFNDA in Fig. 3, are shown in (1).

$$\begin{cases} L \frac{di_a}{dt} + u_{DN} - u_{EN} - L \frac{di_b}{dt} = u_A - u_B \\ L \frac{di_b}{dt} + u_{EN} - u_{FN} - L \frac{di_c}{dt} = u_B - u_C \\ L \frac{di_c}{dt} + u_{FN} - u_{DN} - L \frac{di_a}{dt} = u_C - u_A \end{cases} \quad (1)$$

Switching function is shown in (2). Taking A phase for example, when the above diode is turned on, the d_a^* is 1 value and u_{DN} equal to U_d . When the below diode is turned on, the d_a^* is 0 value and u_{DN} equal to zero. So B phase or C phase is the same program. Accordingly, Equation (3) can be derived.

$$d_k^* = \begin{cases} 1 \\ 0 \end{cases} \quad (k = a, b, c) \quad (2)$$

Where d_k^* is the description of switch status.

$$\begin{cases} u_{DN} = d_a^* U_d \\ u_{EN} = d_b^* U_d \\ u_{FN} = d_c^* U_d \end{cases} \quad (3)$$

If the (3) is substituted into (1), (4) can be derived.

$$\begin{cases} L \frac{di_a}{dt} - L \frac{di_b}{dt} = -(d_a^* - d_b^*) U_d + u_A - u_B \\ L \frac{di_b}{dt} - L \frac{di_c}{dt} = -(d_b^* - d_c^*) U_d + u_B - u_C \\ L \frac{di_c}{dt} - L \frac{di_a}{dt} = -(d_c^* - d_a^*) U_d + u_C - u_A \end{cases} \quad (4)$$

The capacitor voltage equation represented by the switching function of the (5).

$$C \frac{dU_d}{dt} = i_a d_a^* + i_b d_b^* + i_c d_c^* \quad (5)$$

The duty cycle of device S_a, S_b, S_c are the d_a, d_b, d_c which switching pulse signal during a switching cycle. As described in (6).

$$d_k = \frac{t_k}{T_S} \quad (k = a, b, c) \quad (6)$$

During the duty cycle, d_a, d_b and d_c is equal to the switching function the average of d_a^*, d_b^* and d_c^* respectively. When the frequency of switching is relative high, the average sense available d_a, d_b, d_c instead the d_a^*, d_b^*, d_c^* .

The Equation (4) and Equation (5) are transformed to matrix form respectively. The Equation (7) indicates deadbeat current control mathematical model of the inverter.

$$\begin{bmatrix} L & -L & 0 & 0 \\ 0 & L & -L & 0 \\ 0 & 0 & 0 & U_d \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \\ U_d \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -(d_a - d_b)U_d \\ 0 & 0 & 0 & -(d_b - d_c)U_d \\ d_a & d_b & d_c & 0 \end{bmatrix} \times \begin{bmatrix} i_a \\ i_b \\ i_c \\ U_d \end{bmatrix} \quad (7)$$

$$+ \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} u_a \\ u_b \\ u_c \\ 0 \end{bmatrix}$$

If the (7) is discrete, taking ΔT finite increment instead approaches zero the limit of zero. when the switching frequency is relatively high, ΔT can be instead of T_s . That is d_i equal to ΔT , T_s . So the (8) can be derived.

$$\frac{di_k}{dt} = \frac{i_k'' - i_k}{T_s}, (k = a, b, c) \quad (8)$$

Where T_s is the time of switching period, i_k is the actual output current of the k phase in the inverter, i_k'' is k phase compensation current value.

If the (8) is substituted into (7), thus (9) can be derived.

$$\begin{cases} d_a = \frac{1}{3U_d} \left[\frac{L}{T_s} (-2x_a + x_b + x_c) + (2u_A - u_B + u_C) \right] + \frac{1}{2} \\ d_b = \frac{1}{3U_d} \left[\frac{L}{T_s} (x_a - 2x_b + x_c) + (u_A - 2u_B + u_C) \right] + \frac{1}{2} \\ d_c = \frac{1}{3U_d} \left[\frac{L}{T_s} (x_a + x_b - 2x_c) + (u_A + 2u_B + 2u_C) \right] + \frac{1}{2} \end{cases} \quad (9)$$

Where $x_a = i_a'' - i_a$, $x_b = i_b'' - i_b$, $x_c = i_c'' - i_c$.

The d_a , d_b and d_c can be use to control the IGBT devices. The PV grid connected inverter output current i_k is equal to the compensation current i_k'' in a switching cycle.

V. SIMULATION AND ANALYSIS

Deadbeat control algorithm is applied in PV grid connected inverter analysis, and the power is 15kW. In full load state, the grid voltage, current, the waveform distortion rate of grid connected current are researched.

The Fig.4 indicated the grid voltage waveform in full load, and Fig.5 indicated the grid current waveform in full load. The grid current distortion rate of only 1.4% distortion rate can be seen from the Fig.6, which is very small. As can be seen from Fig.7, the grid power factor is

reached to 1.0, that is issued by the current is 100% active current. But the reactive power 0 is inaccurate in Fig.7. The actual power factor of this system is 0.997 through calculation of the total active power 14.09KW and the apparent power 14.13KW.

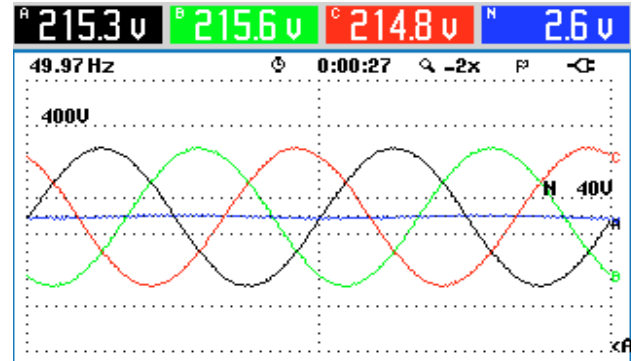


Figure 4. Grid voltage waveform in full load

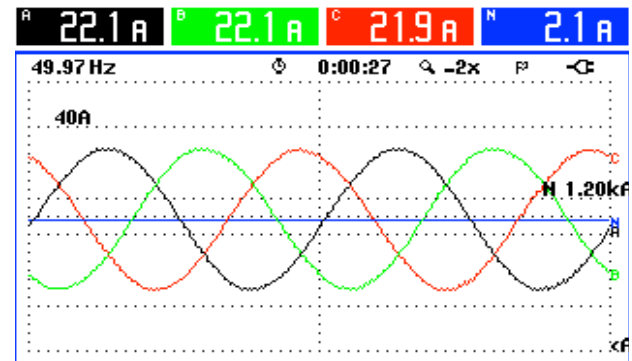


Figure 5. Grid current waveform in full load

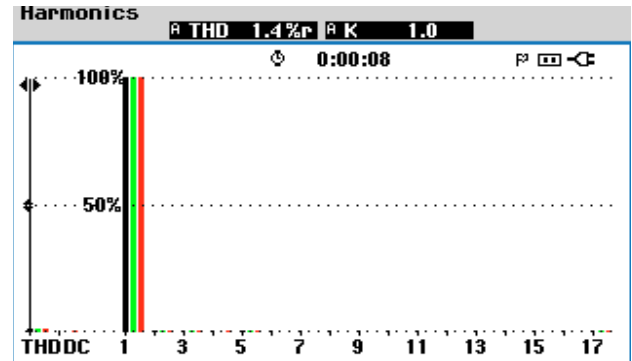


Figure 6. Distortion rate of Grid current in full load

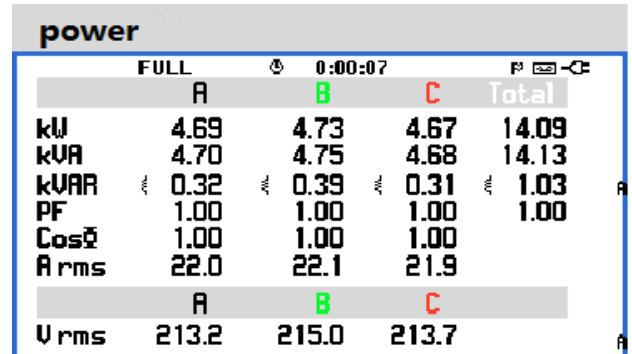


Figure 7. Grid power chart in full load

When the light intensity decreases, the power generation is in the case of 50% of the power. Fig.8 indicated Grid voltage waveform in 50% load. Fig.9 indicated Grid current waveform in 50% load. Fig.10 shows indicated Distortion rate of Grid current waveform in 50% load. The Fig.11 indicated the chart of power generation grid power in 50% load.

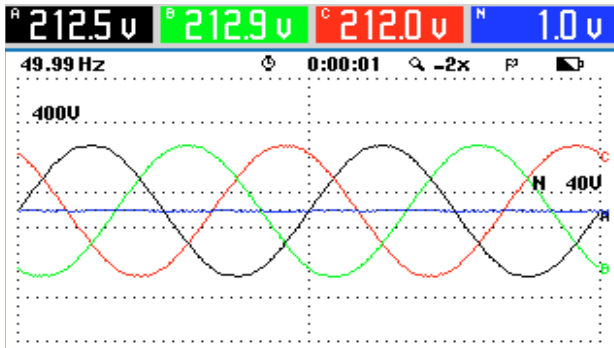


Figure 8. Grid voltage waveform in 50% load

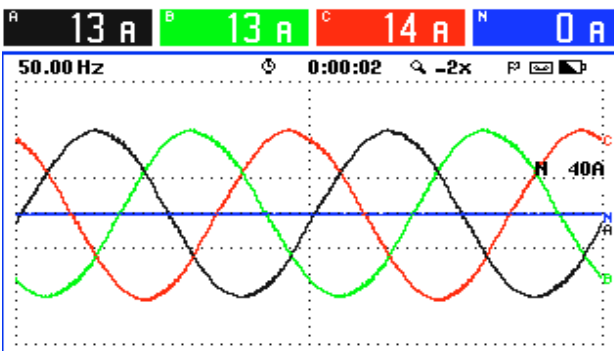


Figure 9. Grid current waveform in 50% load

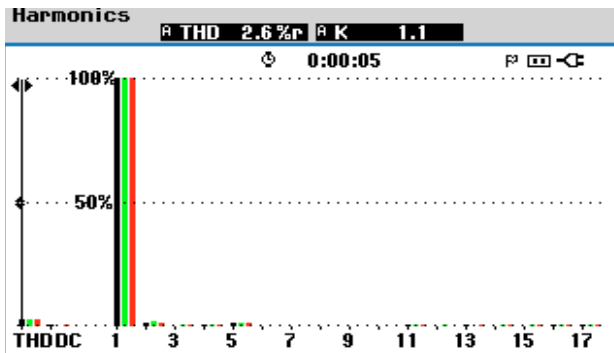


Figure 10. Distortion rate of Grid current in 50% load

power					
	FULL	A	B	C	Total
kW	2.83	2.84	2.85		8.52
kVA	2.85	2.86	2.87		8.57
kVAR	0.33	0.32	0.34		0.98
PF	0.99	0.99	0.99		0.99
Cosφ	1.00	1.00	0.99		0.99
A _{rms}	13.4	13.4	13.5		
	A	B	C		
V _{rms}	212.7	213.2	212.3		

Figure 11. Grid power chart in 50% load

It is no difference between voltage waveform in Fig.8 and Fig.4, because the grid for this small system is an infinite system, also the voltage of the system will not change. As can be seen from the Fig.9, the valid values of current dropped by half, but the sinusoidal waveform of grid current is still well. The distortion rate of grid current waveform is 2.4%, which can be seen in Fig.10. The Fig.11 indicated the grid power factor is 0.99 at this time of the system.

VI. CONCLUSIONS

The deadbeat control algorithm as the current closed-loop control algorithm has high control accuracy, fast dynamic response characteristics to meet the photovoltaic power generation control system requirements. According to the analysis of PV grid connected inverter system, which Power is 15KW. The results indicated the deadbeat control algorithm is effective to control three phase grid output current of the inverter. However, deadbeat control algorithm has limitations, as follows.

(1) It is depend on accurate mathematical model, circuit model based on the system state equations. Also the control degree of accuracy of the effect depends on the parameters of model, so the deviation of the model parameters will lead to the unstable region caused shock.

(2) The maximum duty of output pulse width cycle is restricted, because of sampling and calculation delay. Therefore, the pulse width must be shot when is calculated. If the delay time of the control cycle quite deadbeat control algorithm, deadbeat control can not be achieved in shot output state. The impact of the delay is getting smaller and smaller, because of the high frequency digital signal processor. It has been widely used in sampling and calculation of power electronics control.

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