Novel Design of a Digital PLL for Power Reduction

https://doi.org/10.3991/ijoe.v18i07.30033

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Abstract—Very large-scale integration (VLSI) circuits operating at ultra-low power are currently acquiring more attention from the research group and the industries too. The energy efficient sensor nodes with reduced size are much preferred among applications such as wireless sensor networks, pollution and plant monitoring. The biggest challenge faced by the VLSI designers in present day life is designing a product of new generation which operates on minimum possible power. As an operational gadget, the PLL has wide scope of utilization in media transmission, PCs and electronic applications for jitter reduction, clock synthesis, synchronization etc. As a result, a PLL that can function in the GHz range while consuming less power is required. In this paper, designing and analysis of PLL with numerous outputs has been proposed to be implemented by changing the closed loop frequency control framework PLL blocks. As such, highly effective, low power, ideal area chip can be used for PLL with four various yields as PLL 8x, PLL 4x, PLL 2x and PLL 1x with different frequencies separately. Likewise, it is planned to utilize multi-threshold technique to minimize the leakage current in the circuit. Further, the performance verification of various parameters of PLL are done to acquire negligible power. Direct toolbox YALMIP is used as programming solver as an optimization tool. In addition to this, another method of non-dominated sorting genetic algorithm (NSGA-II) Correlation for optimization is also introduced between both the strategies to find the best outcomes.

Keywords—PLL, NSGA-II, optimization, average power, leakage power, oscillating frequency

1 Introduction

The greatest challenge looked by the VLSI creators today is structuring a new product which provides least power. For preserving the power, it is required to achieve high performance or minimal area. The power consideration is the eventual design criteria in different real-life applications like wristwatches, mobile phones, etc. The main objective of all these applications is minimal power and utmost possible battery lifetime. Low power design was required to reduce the power of the high-performance systems (Bellaouar, Elmasry, 1995).

PLL is found to be a feedback system in which the input signals given externally are phase locked with the produced output signals. Tracking of input signals in frequency

and phase is done by PLL. Some of the applications of PLL include tracking filter, frequency shifting decoding for demodulation of carrier frequencies etc. The digital PLL is one of the types of PLL which uses both combinations of digital as well as analog techniques to achieve powerful operation of the devices (Akila, 2004). Scaling of CMOS devices, has led the digital Phase locked loop (PLL) to increase its market share in wi-fi trans-receivers.

There are two types of digital PLLs discovered since past few years: **Fractional N divider digital PLL** and **Counter-based digital PLL** (Maffezzoni, P., Marucci, G., Levantino, S., & Samori, C. 2013). Counter-based PLLs are commonly utilised in WPAN (Wireless Personal Area Network) applications. Traditional counter-based PLLs, on the other hand, conduct frequency digitization using a high-speed counter and a TDC (time to digital converter). In practical digital circuits, power dissipation is caused due to signal transition, short circuit current and leakage currents. For now, as the technology grows, short circuit and leakage currents have become the main concern (Kao, Chandrakasan 2000; Sirisantana, 2000).

The growth of competitive market sectors like wireless applications depends on the power dissipation as the most critical criterion since the growth rate of the batteries is not convincing. Thus, the power optimization is considered as an essential factor. By concentrated planning, skew will surpass only one information clock period which causes failure and meta-steadiness issues inside sampling process. Though fully synthesis standard-cell libraries have prompted extravagant power usage for ultra-low power genuine applications. The real test is selecting the right True Single-Phase Clock (TSPC) structure for the correct place.

In VLSI circuits operating at ultra-low power, the performance majorly depends on:

- Size of the sensor node
- Energy consumption

In this way these circuits have wide applications in remote sensor network, pollution, biomedical and so forth. For remote applications, power dissipation is extremely pivotal since development rate of batteries isn't persuading. Thus, power optimization is a must. In this present work, the optimization of parameters has been done using the MATLAB software tool. In this work the objective problem is solved with the YALMIP toolbox. It is an optimization tool which has many solvers capable of handling different kind of problems (say Linear problem, Integer Problems, Quadratic problems, quadratically constrained quadratic problems, etc,). Likewise, NSGA-II (genetic algorithm) is additionally utilized for optimization and the correlation of performance parameters is made based on both the methods.

2 Schematic designs

2.1 Phase locked loop design

PLLs includes: Phase frequency detector (PFD), Charge Pump (CP), Low Pass filter (LPF), Current starved voltage-controlled oscillator (CS-VCO) and a divider. The suggested PLL schematic is presented in Figure 1. Similarly, with CS-VCO, the PFD compares the feedback and information signals to generate the error signal. The charge pump and low pass filter are employed to reduce disturbances at the CS-VCO input, resulting in a smoother and crisper signal at the CS-VCO yield. The phase error output of a PFD is routed to a charge pump, which integrates the signal to generate a sharper and smoother signal, minimizing the disturbances at the oscillator's input, forming a PLL. Schematic diagram of each block of PLL is designed using Cadence to get the transient responses.

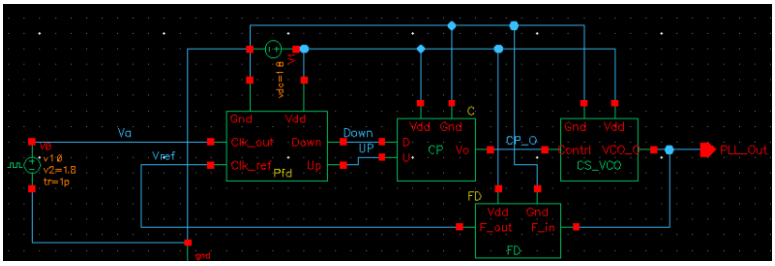

Fig. 1. Schematic diagram of phase locked loop

2.2 Loop filter and charge pump

The charge pump is the circuit that converts the PFD's UP and DOWN signals into a voltage that controls the VCO. The charge pump, as illustrated in Figure 2, comprises of two switched current sources driving a capacitive load. The PFD output signals UP and DOWN turn on and off the charge pump. The charge pump, which has output signals UP and DN, is shown in detail in Figure 2. Positive current IPDI passes through the circuit when the UP signal is high, boosting control voltage. Negative current IPDI runs through the circuit when the down signal gets high, lowering the control voltage. The PLL loop filter's planning is critical to the phase locked loop's overall functioning. The circuit sizes and values are carefully chosen here, with a balance struck between the number of needs and the quantity of space available.

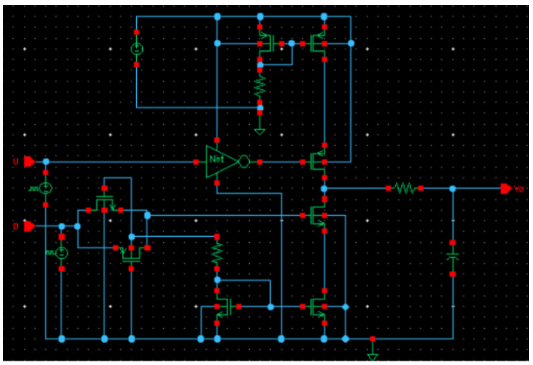

Fig. 2. Schematic of charge pump and loop filter

2.3 Phase frequency detector (PFD)

The phase of two input signals is compared using a phase frequency detector (PFD), which provides a phase error signal. In most situations, it takes two input signals: one from a current-starved voltage-controlled oscillator and one from a reference source. It contains two outputs that inform the remainder of the circuitry what to do to lock onto the phase. Figure 3 depicts the Phase Frequency Detector schematic circuit in detail.

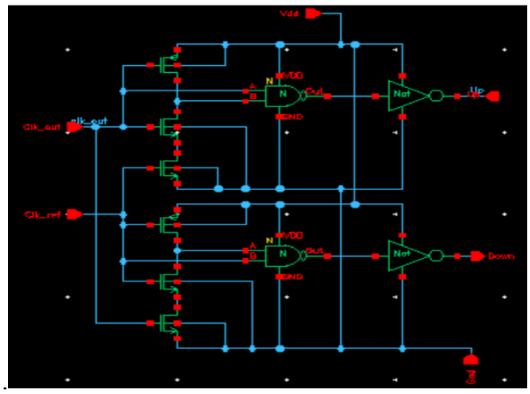

Fig. 3. Schematic of phase frequency detector

2.4 Frequency divider

The VCO frequency is divided by the frequency divider to produce a frequency that is equivalent to the reference frequency. We used a divide-by-two network in this example, but we may change the divider network to synthesize various frequencies. The counter circuit is implemented using two D-flip flops. The frequency divider circuit separates the VCO's clock signal into d-clocks, which are then compared to input data via a phase frequency detector. The schematic outline of the division utilizing the 2-recurrence divider circuit is shown in Figure 4.

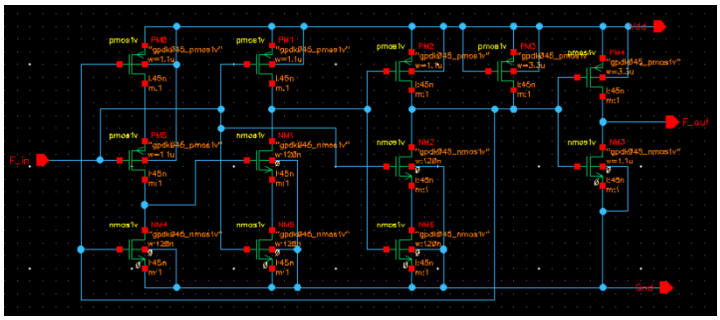

Fig. 4. Schematic diagram of frequency divider

2.5 Current starved inverter VCO

In functioning, the current-starved VCO is comparable to the ring oscillator. Figure 5 shows a five-stage current-starved VCO with PMOS, MP1, and NMOS, MN1 inverters and PMOS, MP6, and NMOS, MN6 current sources. The current sources MP6 and MN6 limit the amount of current available to the inverters MN1 and MP1, resulting in a power-starved inverter. The drain currents of MOSFETs M11 and M12 are identical and are controlled by the input control voltage. In each inverter/current source phase, the currents in MP11 and MN11 are mirrored. Controlling the current via an inverter with a voltage controlled current source is as simple as regulating the charge and discharge time. The control voltage drives this current source, and the current sets the inverter's charge up and discharge times. Because inverters are short on current, the term "current-starved inverter" refers to a topology in which they are permitted to consume. 11 PMOS and 11 PMOS are included in the 5-stage Current Starved Ring Oscillator for Phase Locked Loop (PLL).

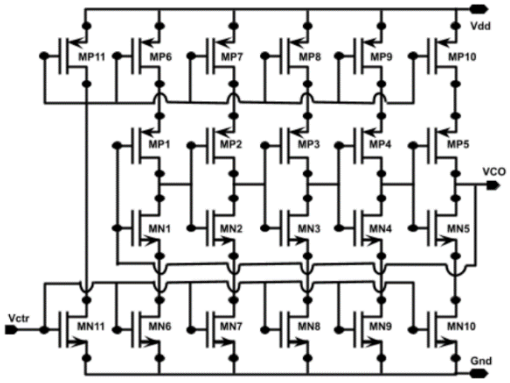

Fig. 5. A five stage current-starved VCO [9]

Figure 6 depicts the five-stage current-starved VCO that was designed. Five cascaded inverters make up the VCO. The schematic for the inverter is shown in Figure 6.

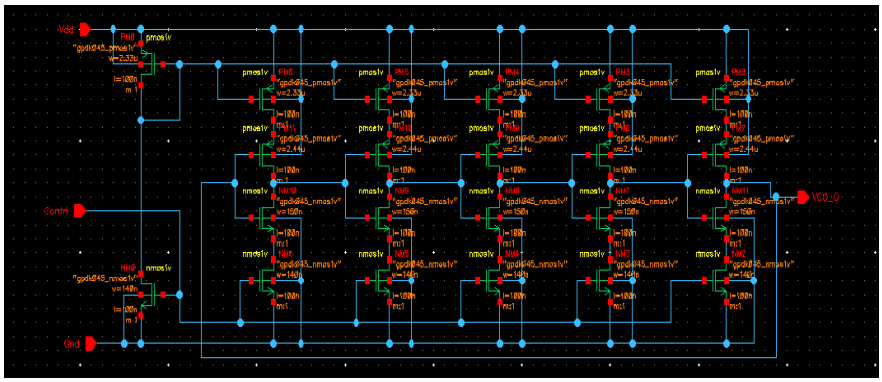

Fig. 6. Schematic diagram of 5-stage current starved VCO

To compute the VCO's operating frequency, the total capacitance (C_{total}) on the drains of the inverter transistors is equal to the sum of the inverter's input (C_{in}) and output capacitances (C_{out}). [8] gives us the total capacitance:

$$C_{total} = (5/2)\, C_{ox}\, (W_P L_P + W_N L_N) \tag{1}$$

Where,

The NMOS transistor width and length are WN and LN, respectively, whereas,

The PMOS transistor width and length are WP and LP, and the gate oxide capacitance per unit area is Cox [8].

$$C_{ox} = \boldsymbol{\varepsilon}_{ox} * \boldsymbol{\varepsilon}_{o} / t_{ox} \tag{2}$$

Where, $\boldsymbol{\varepsilon}_{ox}$ is the permittivity of oxide material (3.9 for SiO2 material),

$\boldsymbol{\varepsilon}_{o}$ free space permittivity (8.854 x 10 -14 F/cm), and

t_{ox} is the oxide thickness

The oscillation frequency of VCO is given by [1]:

$$f_{osc} = I_d / N*C_{total}*V_d \tag{3}$$

Where,

The total number of inverter stages is N.

The oscillation frequency is dependent on total capacitance, number of inverter stages, and current ID, as shown in the above equation. The input voltage Vin can be used to regulate this current. The oscillator's number of stages is chosen; there are five stages.

The CMOS center drain current is computed as follows: [8]:

$$I_D = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \cdot V_{DS}, \text{ for } |V_{DS}| << (V_{GS} - V_T) \tag{4}$$

$\boldsymbol{\mu}$ - mobility of charge carriers

$V_{GS} = V_{in}$, input voltage

$V_{DS} = V_{dd}$, supply voltage

V_T - threshold voltage of transistor

Drain current is found to be directly proportional to gate-phase capacitance. **W/L Ratio is considered as beta.** Each stage is considered as beta. The beta values are optimized first and then the gate oxide thickness. Oscillator frequency is related with gate oxide thickness and beta of the transistors.

In each stage, there are 2 transistors – 1 NMOS & 1 PMOS for current starving and 1 NMOS & 1 PMOS for Invertor. Every stage would be repeating this.

While optimizing there is a need to maintain the average & leakage power. So, these also have been related with gate oxide thickness and then beta1, beta 2, beta 3 ratios. Thus, once these constraints have been designed, YALMIP algorithm is applied for optimizing the frequency of oscillation. Similarly, the same objective function has been optimized with NSGA2 i.e., the comparison algorithm.

3 Optimization of design parameters

According to eq.(3), the frequency of oscillation is inversely proportional to total capacitance and directly proportional to drain current I_d .The appropriate frequency may be achieved by carefully controlling the W/L ratio and the thickness of the oxide layer (t_{ox}). After simulating the relationship between these parameters empirically, the three equivalent model response equations were developed as follows:

1. The frequency response in terms of input voltage is:

$$f_{osc} = 786.43 - 93.36t_{ox} + 60.3\beta_2 \tag{5}$$

2. VCO's total power consumption is:

$$P_{av} = 35.05 + 5.7\beta_4 + 3.3\beta_3 \tag{6}$$

3. The power consumption caused by gate tunnelling current is:

$$P_{leak} = 376.35 - 28.58\ t_{ox} + 29.32\beta_1 + 36.17\beta_2 \tag{7}$$

Where,

PMOS inverter transistors have a W/L ratio = β_1,

NMOS inverter transistors have a W/L ratio = β_2,

PMOS current starve transistors have a W/L ratio = β_3 and

NMOS current starve transistors have a W/L ratio = β_4.

To prevent the design rule mistake, the above objectives were optimized with the following constraints:

$$1.4\ \text{nm} \le t_{ox} \le 1.7\ \text{nm}$$
$$5 \le \beta_1 \le 10$$
$$1.72 \le \beta_2 \le 3.44$$
$$5 \le \beta_3 \le 10$$
$$1.72 \le \beta_4 \le 3.44$$

Since there are three objectives with five variables, obtaining the best solutions with less time is a difficult task in the design of experiments (DOE) methods. In this work, a multi-objective optimization method is converted to a single objective function which is maximizing the oscillation frequency f_{osc}. The remaining two objectives are converted to new constraints so that we can maintain the **Leakage power (P_{leak})** and the maximum **Dissipation power (P_{av})**.

The modified objective problem and constraints for YALMIP tool are:

$$\begin{gathered}\text{Max} \\ t_{ox},\beta_1,\beta_2,\beta_3,\beta_4 \\ F_{osc} \\ \text{Subject to,} \\ 1.4\text{ nm} \le t_{ox} \le 1.7\text{ nm} \\ 5 \le \beta_1 \le 10 \\ 1.72 \le \beta_2 \le 3.44 \\ 5 \le \beta_3 \le 10 \\ 1.72 \le \beta_4 \le 3.44 \\ P_{av} <= 70\mu\text{ W} \\ P_{leak} <= 600\text{p W}\end{gathered}$$

The optimization of parameters has been done using the MATLAB software tool. In this work the objective problem is solved with the YALMIP toolbox. It is an optimization tool which has many solvers capable of handling different kind of problems (say Linear problem, Integer Problems, Quadratic problems, quadratically constrained quadratic problems, etc.,).

4 NSGA-II - Non-dominated sorting genetic algorithm

The problem was also handled using a non-domination based genetic algorithm as a comparison study (NSGA-II). As is typical, the population is initialized. After it has been released, the populace is divided into fronts based on non-domination. The first front is no longer dominating in today's population, but the second front is dominated entirely by people from the first front, and so on. Each front's members are given a rank (fitness) grade based on the front they belong to. The first row is assigned a fitness value of one, the second row is assigned a fitness value of two, and so on. For each person, a new metric called crowding distance is calculated in addition to the fitness value. A person's crowding distance is the distance between them and their neighbors. A large average crowding distance will result in more population variation.

Binary tournament selection is used to pick parents from the population based on rank and crowding distance. If a person's rank is lower or the crowding distance is larger, they are chosen. Crossover and mutation operators produce offspring in the chosen population, which will be explained in depth in the following section. Only the best N individuals are selected from the existing population and progeny, which are then sorted again by non-domination. On the last front, the choice is made based on rank and crowding distance. This NSGA II's multi-objective optimization problem is:

$$\max_{tox,\beta1,\beta2,\beta3,\beta4} Fosc$$

$$\min_{tox,\beta1,\beta2,\beta3,\beta4} Pavg$$

$$\min_{tox,\beta1,\beta2,\beta3,\beta4} Pleak$$

Subject to,

1.4 nm ≤ Tox ≤ 1.7 nm
$5 \le \beta_1 \le 10$
$1.72 \le \beta_2 \le 3.44$
$5 \le \beta_3 \le 10$
$1.72 \le \beta_4 \le 3.44$

5 Results

Figure 7 shows the output signal of the VCO at a control voltage of VDD/2. The supply voltage is tested between 1.1 and 1.8 V.

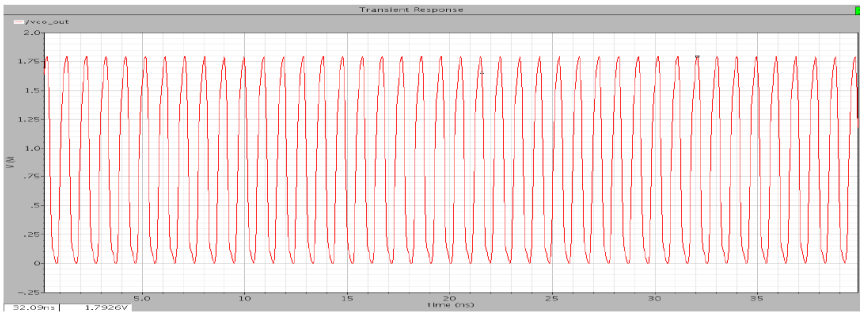

Fig. 7. Output signal of the VCO

In Figure 8, the characteristics of Voltage controlled oscillator are shown. A clear graph between the input voltage (Vin) and VCO frequency is depicted in the graph. The overall power consumption is depending on the input voltage of VCO.

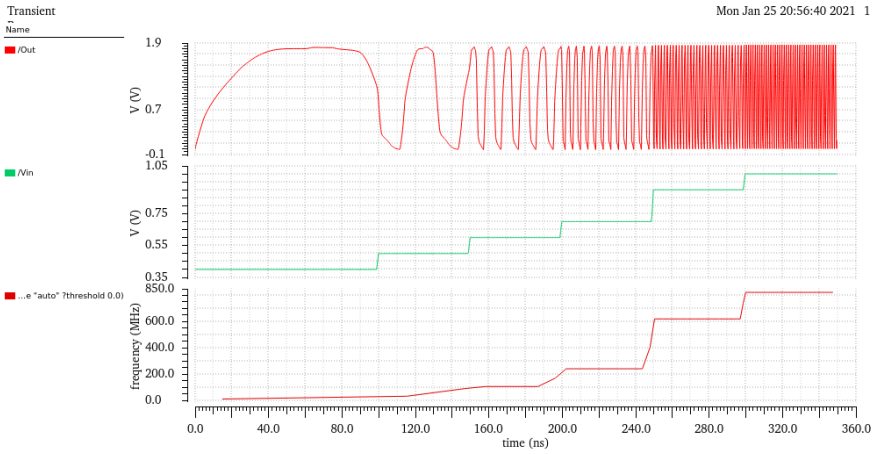

Fig. 8. Simulation result for VCO

In Figure 9, power vs input voltage curve is shown which depicts that, if input voltage increases then the operating frequency will be increased. So, power will be increased. Thus, in order to get low power, it is required to maintain less operating frequency and input voltage. Also, by putting sleep transistor below the threshold voltage and using it, in addition to reducing power consumption, the bandwidth if the loo is also reduced.

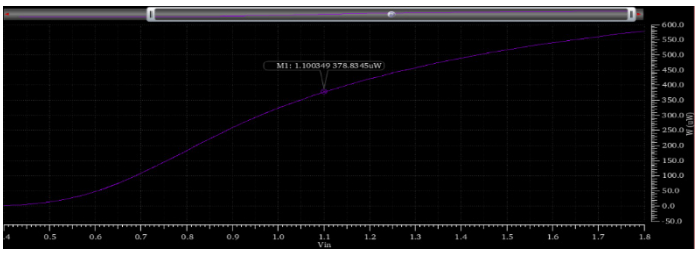

Fig. 9. Power vs input voltage of VCO

5.1 Simulation results

The optimum values of design parameters obtained from the simulation are,

$$\beta_1 = 5,$$
$$\beta_2 = 3.44,$$
$$\beta_3 = 5,$$
$$\beta_4 = 1.72,$$
$$t_{ox} = 1.4\text{nm}$$

The optimization using the NSGA-II genetic algorithm is found to be as shown in Figure 10.

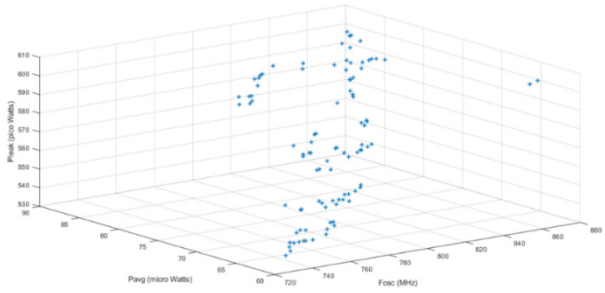

Fig. 10. Optimization using genetic algorithm

While comparing the final results obtained from YALMIP and NSGA-II, the obtained values of the parameters are as compared and shown in the following Table 1.

Table 1. Comparison of parameters obtained from YALMIP & NSGA-II

PARAMETER	YALMIP	NSGA_II
Beta1 (β_1)	5	5.00005808
Beta2 (β_2)	3.44	2.53049527
Beta3 (β_3)	5	9.707991203
Beta4 (β_4)	1.72	3.038341177
t_{ox}	1.4	1.4
F_{osc} (MHz)	863.158	808.3148648
P_{avg} (μW)	61.354	84.40491568
P_{leak} (pW)	607.3628	574.4677168

Both techniques provide distinct value possibilities for the variable that has to be optimized. The algorithm then assesses the objective function and attempts to obtain the optimal output for those variables in order to ensure that the oscillation frequency is high and that power limitations are met. The major goal is to improve the transistor's W/L (beta) ratio.

The oscillation frequency was discovered to be **863.158MHz** prior to optimization. The oscillation frequency was lowered to 808.314MHz after applying the genetic optimization technique to this circuit. After optimization, the average power (P_{avg}) increased to **84.4049μW**, while the leakage power (P_{leak}) fell to **574.467pW**.

6 Conclusion

The current-starved voltage-controlled oscillator (VCO) in this work produces a frequency of 863MHz. Due to the widespread usage of phase locked loop (PLL) in wireless communication systems, any desired frequency may be created based on application needs. The size of the transistors determines the center frequency of oscillation of the VCO. By choosing transistor sizes carefully, the frequency variation from the target

value may be decreased. The major goal of the digitally controlled oscillator is to provide high frequency while using minimal power. The W/L ratios of transistors are optimized for this. Two optimization approaches for study of an objective function, maximizing of oscillation frequency with power limitations are presented in this work.

Each approach has its own set of optimization requirements. The YALMIP approach has a higher leakage power than the NSGA II optimization algorithm, but it delivers the highest oscillation frequency. The leakage power, on the other hand, is lower in the NSGA II algorithm, which has a high average power and low oscillation frequency. The NSGA-II genetic algorithm technique is used to minimize leakage power, using frequency of oscillation as the primary target function. Table 2 compares the performance of classical programming, geometric programming, and the NSGA-II method in this study.

Table 2. Performance comparison of present research with already existing work

FACTOR	CS-VCO USING TRADITIONAL METHOD	[1]	[2]	CURRENT WORK
Frequency(f)	1.012GHz	1.0000457GHz	1.012 GHz	863 MHz
Power(P)	432.456µW	539.65µW	386.64 µW	61µW
Phase Noise @1GHz offset				
Phase Noise @ 1MHz offset	-	-	-138 dBc/Hz	- 143 dBc/Hz
	-82.7 dBc/Hz	-82.6 dBc/Hz	-	-71.41 dBc/Hz

As a result of the unique PLL design, it has been discovered that the parameters can be optimized using the NSGA-II algorithm to produce the lowest leakage power, making the PLL circuit the best for usage.

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Article submitted 2022-02-07. Resubmitted 2022-04-02. Final acceptance 2022-04-02. Final version published as submitted by the authors.