Basic Concepts of a Phase-Locked Loop Control System

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Abstract—Phase-locked loop (PLL) is one of the main components of modern electronic design and has been around for a considerable number of years. It is a technique that has greatly contributed to the technological advancement of communications and control systems. This paper presents a phase-locked loop tutorial based on a control system, it gives a concise review of basic concepts, the different types of PLLs, linear analysis approaches of analog systems PLL is discussed, furthermore the theoretical analysis of the steady-state error in detail is presented, and its simulations of different phase offset values in C program are presented, and show how the response of the loop changes.

Keywords—phase-locked loop, phase error, steady-state

1 Introduction

The phase-locked loop control systems were invented in the early part of the twentieth century [1], [2], and are now extensively used in advanced telecommunications and computers, Richman was the first researcher to have completed equations defining the capture period for a phase-locked loop of the first order [3]. A study document outlines some of the histories of analog loops by Gupta [1].

Phase-locked loops (PLLs) are one of the basic components of modern electronic systems, PLLs have enabled important progress in the processing of signals in the frequency domain. They are now widely used in modern telecommunications and computers, as well as in many other applications, computer architectures [4], gyroscope systems [5], GPS navigation [6].

Work on digital PLLs is driven by the steady supply of components that offer advantages over conventional components [7], the concept of the PLL system was clearly defined and well-established [7]. Prior to the invention of integrated PLL, the systems were very complex and expensive for use in most manufacturing systems. Nowadays, PLL integrated circuits are manufactured at a very low cost. PLL technology emerged when integrated circuits supported many radio functions. PLL can easily be integrated into the radio by simply appending a number of additional circuits to the IC. Since 1970, phase-locked loop control systems have been quickly advanced for AC and DC motor control systems based on analog PLL integrated circuits IC [9–11].

These basic concepts approach PLL from the control designer's point of view. The purpose of this paper is to map out the control design of PLL. The paper is organized

as follows: Section 2 presents an analysis of a PLL structure. Section 3 presents various types of PLL. Section 4 develops a small signal error of PLL and discusses the performance of tracking phase error, and shows the basic characteristics of the transfer function for the loop stability. Section 5 discusses the important order of the PLL for the stability of the loop and we present a simulation with different phase offset values. Section 6 presents the dynamic limit range of PLL. Finally, section 7 presents conclusion.

2 Analysis of a PLL structure

PLL is composed of three main functional units: Phase detector (PD) or comparator, low pass filter (LPF), voltage controlled oscillator (VCO). A block diagram of an analog PLL is presented in Figure 1. The control variable of the PLL is

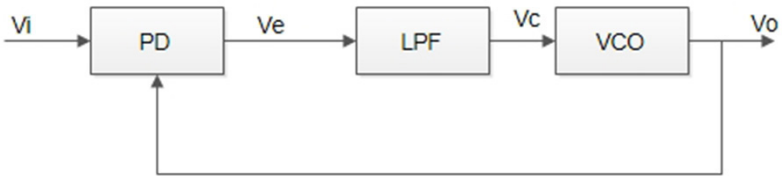

Fig. 1. Block diagram of classical PLL

the phase of an oscillator signal, this phase is monitored by a voltage or current signal and as such, it is referred a voltage or current-controlled oscillator. The input signal of a PLL, as seen in Figure, can be given as follows:

$$V_i(t) = A_i \cos\varphi_i(t) \tag{1}$$

$$V_i(t) = A_i \cos(\omega_i t + \theta_i) \tag{2}$$

without any lack of generalization, we suppose that the VCO output signal in the phase detector is given by:

$$V_o(t) = A_o \cos\varphi_o(t) \tag{3}$$

$$V_o(t) = A_o \cos(\omega_o t + \theta_o) \tag{4}$$

The output of the phase detector in Figure 1 is given by

$$V_e(t) = V_i(t)V_o(t) \tag{5}$$

By using the familiar trigonometric PLL term identity

$$V_e(t) = A_i A_o \cos(\omega_i(t) + \theta_i)\cos(\omega_o(t) + \theta_o) \tag{6}$$

$$V_e(t) = \frac{A_i A_o}{2}\cos((\omega_i + \omega_o)t + \theta_i + \theta_o)\cos((\omega_i - \omega_o)t + \theta_i - \theta_o) \tag{7}$$

as well as a phase detector (PD) are applied to the inputs when the phases are compared. The output (PD) V_e generally consists of two elements:

$$V_e(t) = V_{lpf}(t) + V_{hpf}(t) \tag{8}$$

The first element V_{lpf} is a low-pass frequency waveform, referred to as a difference frequency element, due to its frequency is equivalent to the difference $\omega_i - \omega_o$ in the two signals passed to the phase detector.

Further, the second element V_{hpf} is a high pass frequency, which is defined as the ripple, which depends on the type of phase detector. The basic ripple frequency equals either the sum frequency $\omega_i + \omega_o$ the reference signal frequency ω_i or the VCO signal frequency ω_o.

The output of the phase detector is then passed to the filter (LPF), the LPF performs a dual function, on the one hand, it reduces the waviness and noise that accompany the reference signal, on the other hand, it functions as a control filter to enhance the loop's dynamics.

The V_c output of the LPF passes to the VCO input, depending on the case, the VCO signal is synchronized with the reference signal. We recall that two signals are considered phase-locked or synchronized when their frequencies are identical and their phase error keeps steady.

3 Various types of PLL

The different types of PLL implementation are divided into three general classes:

- Analog PLL: the phase detector (PD) is normally a four-quadrant multiplier and the low pass filter is an analog filter (active or passive), the VCO is a relaxation quasi-harmonic oscillator type [2].
- Mixed PLL: the phase detector is an XOR gate or a digital circuit, a phase-frequency detector (PFD), a Master-Slave flip-flop [12], the VCO is an oscillator and the LPF analog circuit is of the type (active or passive). The essential waveform frequency is equal to the reference frequency, but in the XOR case, it is equivalent to the sum frequency.
- Digital PLL: All components of the system are software or digital circuits [13].

A further categorization of PLLs is according to the value of the steady-state error. This phase error is related to the system's count of integrators in the control loop. Based on the conventional theory of control, the sum of the integrators determines the nature of the system. In classical PLL theory, the type of PLL is as follows:

$$\textit{Type of PLL} = \textit{Number of integrators} + 1$$

All phase-locked loops have a VCO which counts as an integrator, and the type and order have to do with the loop transfer function. In type 1 of PLL, the reference frequency is related to the steady-state phase error, while in type 2 the error is steady and is not related to the reference frequency. In fact, PLLs are differentiated by their order.

Even though PLLs are designed as higher-order systems, they are generally considered to be in order as defined [14]:

$$Order\ of\ PLL = Order\ of\ Low\ pass\ filter + 1$$

Without a filter, the PLL is referred to as a first-order PLL or first-order loop. As an example type 1 order-3 PLL would have a VCO, no charge pump, and a second-order loop filter. The most frequently applied filters are the proportional-integral controller (PI), the phase delay filter, and the phase advance filter.

4 Small error analysis for a classical PLL

In our case, a phase-locked loop is considered a circuit that follows the phase and frequency of an input sinusoidal signal as shown in Figure 2.

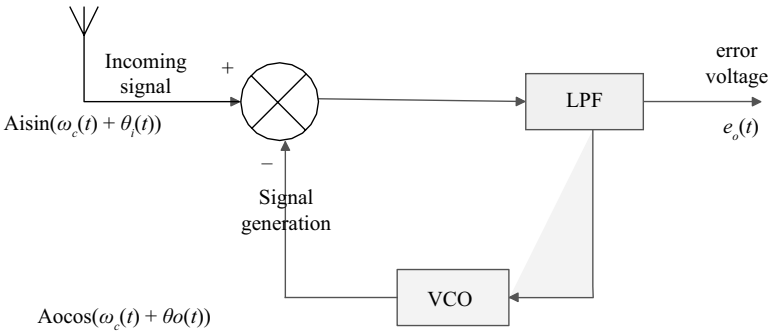

Fig. 2. Feedback loop of PLL

We have two signals:

$$A_i \sin(\omega_o t + \psi(t))$$

and

$$A_o \cos(\omega_c t + \theta_o(t))$$

We rewrite the phase of the input signal in a different way

$$\omega_o t + \psi(t) = \omega_c(t) + (\omega_o - \omega_c)t + \psi(t) \tag{9}$$

$$\omega_o(t) + \psi(t) = \omega_c(t) + \theta_i(t) \tag{10}$$

That finally found

$$A_i \sin(\omega_c(t) + \theta_i(t))$$

and

$$A_o \cos(\omega_c(t) + \theta_o(t))$$

as we know there is a relationship between phase and frequency $\theta(t) = \int \omega(t)dt$, $e_o(t)$ is a error voltage input of VCO [15], as is shown in Figure 3 we have a linear equation

$$\omega(t) = \omega_c(t) + Ce_o(t) \tag{11}$$

Fig. 3. Tracking error of VCO

We note that

$$\dot{\theta}(t) = Ce_o(t) \tag{12}$$

$\omega(t)$ is output frequency of VCO, and if $e_o(t) = 0$ that means in this case $\omega(t) = \omega_c$ Where ω_c is free running frequency.

The following equation is the input to the voltage convolution:

$$e_o(t) = h(t) * \frac{A_i A_o}{2} \sin(\theta_i(t) - \theta_o(t)) \tag{13}$$

$$Ce_o(t) = C\frac{A_i A_o}{2} \int h(t-x) \sin(\theta_i(x) - \theta_o(x))dx \tag{14}$$

Where

$C\frac{A_i A_o}{2} = K$ is the loop gain parameter, then

$$\dot{\theta}(t) = K \int h(t-x) \sin(\theta_i(x) - \theta_o(x))dx \tag{15}$$

This phase difference in s domain is $\theta_i(s) - \theta_o(s)$ is known as the phase error and is denoted by $\theta_e(s)$. Hence

$$\theta_e(s) = \theta_i(s) - \theta_o(s) \tag{16}$$

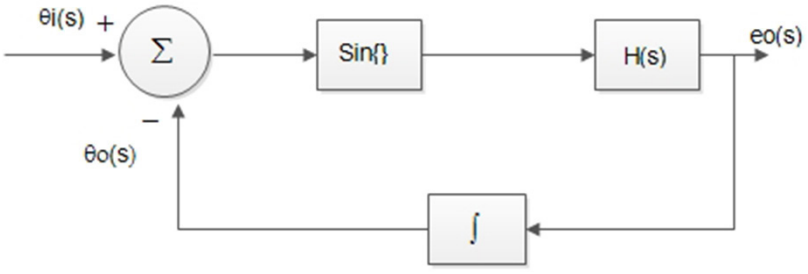

Fig. 4. A non-linear equivalent model of PLL

According to both Figures 2 and 4, we can see that they are similar, except that the multiplier in the equivalent model has been replaced by a subtractor as a phase discriminator and a sinusoidal nonlinearity and the VCO by an integrator. A large number of locked PLLs can be approached as linear. We assume that the error θ_e is small, linear with slow variation:

$$\sin(\theta_e) \approx \theta_e$$

In the balance case, the loop must adjust the control signal θ_e, such as the output θ_o of the VCO is about the same as the phase θ_i, thus through successful operation the phase error θ_e should equal zero.

$$\theta_e(s) > 0 \Rightarrow \theta_i(s) - \theta_o(s) > 0$$

In the first case if θ_e is positive, let's see what can turn it to zero.

– $\theta_i > \theta_o$ so θ_o should increase, and the oscillator of the VCO generates frequency ω:

$$\omega > \omega_c$$

That means this frequency runs rapidly (speed up), so the angle of the sine of the signal entering here follows the angle of the cosine of the signal generated by the VCO until it is equal, and the error is zero.

– $\theta_i < \theta_o$, in this case, θ_o decreases, and the oscillator of the VCO generates frequency ω:

$$\omega < \omega_c$$

Therefore, the oscillator reduces the speed (slows down) until the error is zero. This results from the relationship Input/Output of the phase detector are shown in Figure 5 following the average of the phase error and the phase error. This relationship is known as an S-curve because of its form similar to the English letter "S".

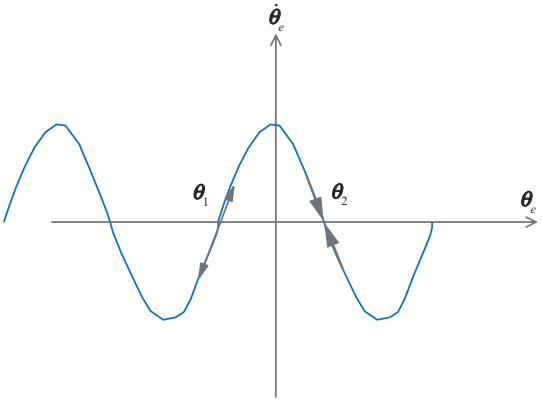

Fig. 5. S-curve of phase detector

It can be observed that the PLL can eliminate even the largest error $\theta_e(s)$. An increase with a larger error θ_e, thus θ_o increases then pulls $\theta_e(s) = \theta_i(s) - \theta_o(s)$ back towards zero.

Nevertheless, the directional force is magnitude dependent of $\dot{\theta}_e(s)$, that is not the same out of the straight-line range (linear function). We can conclude that in the straight-line area as seen in Figure 5:

- A negative gradient near zero will not produce a stable locking point θ_1.
- A positive gradient near zero results in steady state locking θ_2.

The PLL design in Figure 6 is feedback on a closed-loop system. $T(s)$ is the transfer function from reference input to VCO output, it is achieved as follows:

$$T(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{KH(s)\frac{1}{s}}{1 + KH(s)\frac{1}{s}} \tag{17}$$

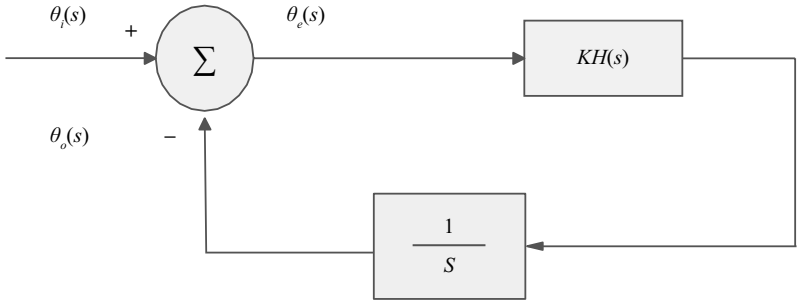

Fig. 6. Linear basic model of the PLL

In the same way, the transfer function of sensitivity between the reference and the phase error is

$$S(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{1}{1 + KH(s)\frac{1}{s}} \tag{18}$$

$$S(s) = \frac{s}{s + KH(s)} \tag{19}$$

The basic requirements for the function are the ordering, the system type, and the stability of the loop. The order of the PLL system should be self-evident from the denominator of the Equation 17, the system can be stable by a number of conventional techniques, such as the following: Bode plots, Nyquist plots, Nicholas charts, and root locus [16].

5 The steady-state error

As seen from Equation 9

$$\theta_i(t) = (\omega_o - \omega_c)t + \psi \tag{20}$$

which is a Laplace transform defined by

$$\theta_i(s) = \frac{(\omega_o - \omega_c)}{s^2} + \frac{\psi}{s} \tag{21}$$

From Equation 19 we can obtained the error

$$\theta_e(s) = \left(\frac{(\omega_o - \omega_c)}{s^2} + \frac{\psi}{s} \right) \left(\frac{s}{s + KH(s)} \right) \tag{22}$$

The steady-state errors of PLLs are generated based on a linear analysis by using the final value theorem in Laplace.

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to o} s\theta_e(s) \tag{23}$$

$$= \lim_{s \to 0} s\theta_i(s)S(s) \tag{24}$$

We assume that the PLL is in the first-order no loop filter, $H(s) = 1$, and the PLL goes in transit stable

$$\lim_{t \to \infty} \theta_e(t) = \frac{(\omega_o - \omega_c)}{K} \tag{25}$$

then the output signal of VCO is

$$A_o \cos(\omega_o(t) + \psi(t) + \frac{(\omega_o - \omega_c)}{K})$$

this term represents phase offset or phase error in the loop

$$\phi_{offset} = \frac{(\omega_o - \omega_c)}{K} \tag{26}$$

So the steady-state phase offset can be controlled by controlling $(\omega_o - \omega_i)$, also to minimize the phase offset or phase error required, the gain K of the PLL loop must be maximized. Hence a high loop gain is beneficial for reducing phase error. Simulations in the **C** program are presented to quickly model the performance of the system. Figures 7, 8 and 9 present the impact of different values of the phase offset of PLL on system performance.

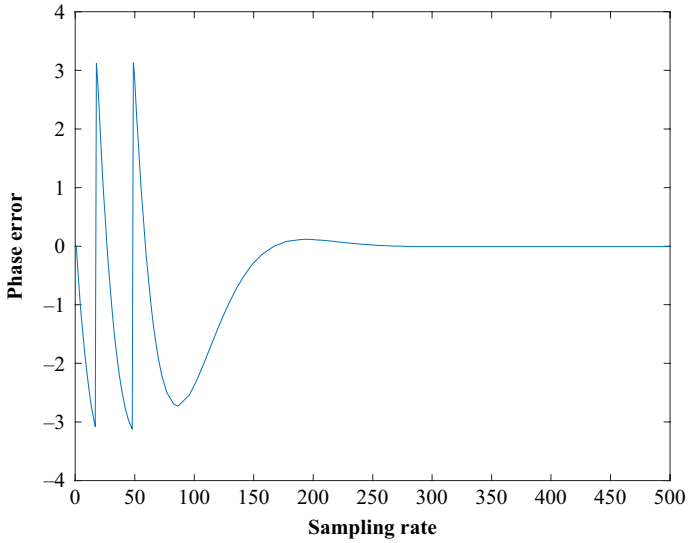

Fig. 7. Locking range of output phase detector at phase offset 0

In the second-order of PLL, the loop filter is $H(s) = \frac{s+a}{s}$

$$\lim_{s \to 0} s\theta_e(s) = 0 \tag{27}$$

then the final output signal of VCO is the same incoming signal that gives

$$A_o \cos(\omega_o(t) + \psi(t))$$

in this case the PLL is more stable than the first-order.

As Equation 21, any PLL consisting of a VCO will be a type 1 system and realize zero steady-state error to a phase step at θ_i.

It should be noted that third-order PLLs and the design of high-order PLLs are getting more and more attention in deep space communication and demand very-high throughput clock recovery in serial data communications [17].

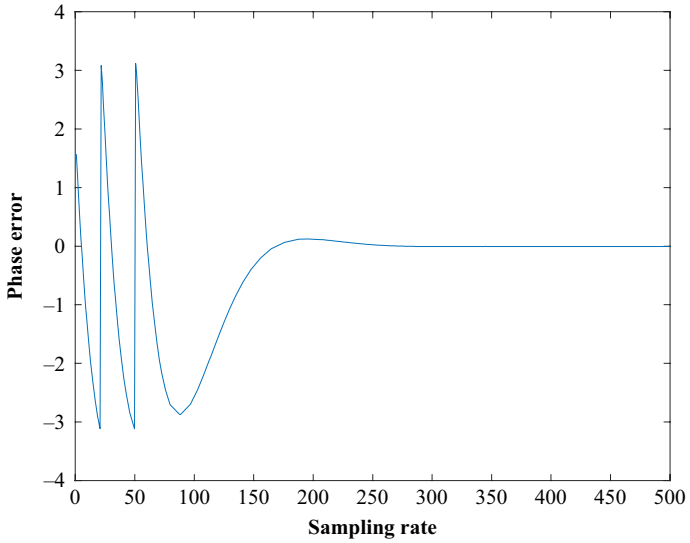

Fig. 8. Locking range of output phase detector at phase offset $\frac{\pi}{2}$

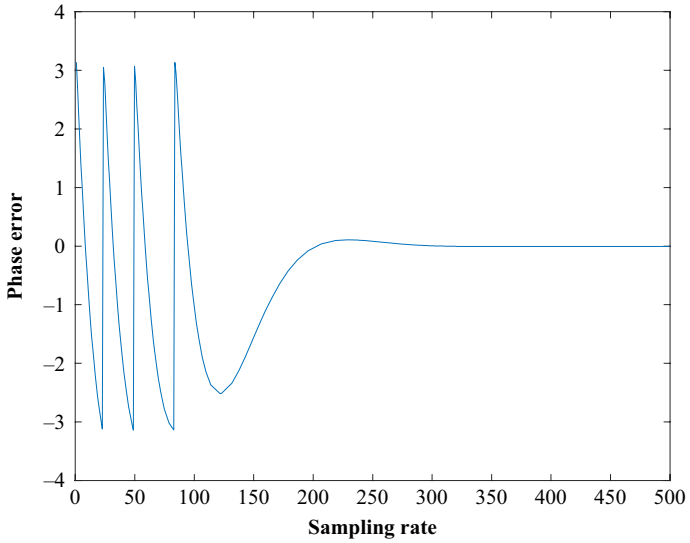

Fig. 9. Locking range of output phase detector at phase offset π

6 PLL dynamic limit ranges

6.1 The holding range

The PLL is able to maintain the stability of the phase tracking, its frequency range is defined as the holding range $\Delta\omega_H$. This is identified by computing the offset of the reference input frequency that causes the phase difference to fall outside the linear analysis. The holding range of control is as follows:

$$\Delta\omega_H = KH(0)$$

When the input frequency is closely enough related to that of the VCO, it locks with only a phase shift, no cycle slip occurs before locking [8].

6.2 The locking range

The locking range $\Delta\omega_L$, is identified as the frequency range where the PLL achieves the phase-locked condition [18]. In the second or higher-order loops, the locking range is always less than the holding range as shown in Figure 10, but

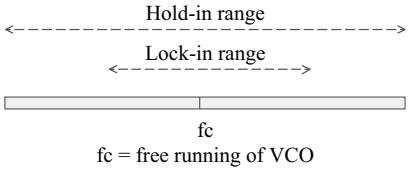

Fig. 10. Dynamic limit ranges of a PLL

in case the loop is of the first order, the locking range is the same as the holding range.

Several cases may arise depending on the original frequency difference of both signals.

If $|\omega_i - \omega_o| > \Delta\omega_L$, the circuit will tend to get progressively locked, presenting a cycle jump. This condition usually has the disadvantage of lasting too long. If the loop is not going to converge, the condition turns into an unlimited length. This situation must therefore be completely avoided during normal operating conditions.

If, on the other hand $|\omega_i - \omega_o| < \Delta\omega_L$, then the output signal of the PLL device accurately tracks the phase and/or frequency variation of the input signal these are the best working requirements.

7 Conclusion

This paper is an investigation of the design and performance analysis of a Phase-Locked Loop circuit device and its application in different technological fields particularity in control and communication systems, and provides a concise study of the literature and reported work in PLL design, and also discusses the steady-state error and

analysis. The small linear error of the output phase detector presents the performance in the tracking phase of a reference signal, shown by the C program with different values of phase offset. Finally, it is necessary to note: A PLL that lacks a filter (naturally called a first-order PLL) is even applied in certain implementations in which noise is not a major problem and a higher-order loop filter can eliminate spurs, but raising the order also raises the phase offset of these filters, which makes them susceptible to instability.

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