Design and Analysis of High Performance Frequency Divider in 32 nm CMOS Technology for Biomedical Applications

https://doi.org/10.3991/ijoe.v19i07.39145

Sanjay Grewal, Owais Ahmad Shah(✉)
Department of Electronics & Communication Engineering, Noida International University, Gautam Budh Nagar, Uttar Pradesh, India
mail_owais@yahoo.co.in

Abstract—In this paper, a 3-bit frequency divider (FD) using a novel sense amplifier based flip-flop (SAFF) is presented and demonstrated. The delay in this design was meticulously improved resulting in better values of power delay product (PDP).The latching stage of the proposed design makes use of a novel single ended structure. Comparative analysis in 32 nm CMOS technology using T-SPICE revealed significant and quantitative differences between the proposed design and the existing designs. The PDP results were obtained for ±10% voltage variation, wide temperature range of −40 °C to 125 °C and at extreme corner cases. Results indicated that the PDP of the new design at nominal operating conditions decreased by minimum of 27.28% and maximum of 57.49%. The proposed design was also at par with available design in terms of area and power. The analysis on the FD proved the assertions that the proposed design is a feasible alternative for high performance applications.

Keywords—low power design, CMOS digital circuit, high speed, sense amplifier based flip-flop, counter

1 Introduction

Almost all modern digital very large scale integration (VLSI) circuits rely on flip flops as their most fundamental building element [1]. In addition to ensuring the chip's proper timing, functionality, and performance, they also account for a significant portion of the chip's overall power consumption. Therefore, it can be said that the power consumption of the circuit is directly related to the architecture of the flip-flops used in the circuit. As a result, it's crucial to cut down on the circuit's overall power usage by designing ultra-low power flip-flops [2].

Flip-flops (FFs) have a wide range of potential uses in the development of low-power and high performance biomedical applications. Systems like Pacemaker rely on flip-flops for the smooth functioning of their many specialized modules, such as analog to digital converters (ADC), comparators, filters, sample and hold circuits, and more. Efforts are currently being made to deploy ADCs based on the successive

approximation register (SAR) design, which will result in even greater power savings due to the elimination of the need for active analogue circuitry [3].

Additionally, in medical science, surface electrodes allow for the acquisition of electrical signals from the heart, brain, and muscles. These signals are known as Electrocardiograms (ECGs), Electroencephalograms (EEGs), and Electromyograms (EMGs), respectively. The characteristic currents generated by the heart's contracting and relaxing cardiac muscle translate into a voltage on the skin's surface in ECG. The signal's peaks (or waves) may be interpreted as representing the atrial and ventricular walls contracting and relaxing. ECGs often fall between the frequency ranges of 0.05 Hz to 100 Hz [4]. The EEG is created at the surface of the scalp as a result of the activity of nerve cells in the brain, which demonstrates the on-going electrical oscillations [5]. Electrical activity of contracting muscles just beneath the skin's surface is what causes the EMG to be recorded at the skin's surface. In certain cases, the EMG frequency may exceed 10,000 Hz [6]. The aforementioned three signals are all analogue in nature, necessitating the usage of ADCs to convert them to their digital equivalents.

One of the important components of an ADC circuit for setting a target frequency can be a frequency divider. The purpose of the circuit is to split the high frequency signal in order to get the lower frequency signal for a particular frequency value by dropping the frequency of the high frequency signal [7]. The frequency divider circuit has numerous possible uses. Creating a 1 MHz clock pulse from a 50 MHz input is one example. A 230 V 50 Hz sine wave AC signal is first converted to a 5 V 50 Hz sine wave AC signal then using standard opamp circuitry, it was changed into a 5 V, 50 Hz square wave signal. Once the signal has been lowered to 50 Hz, it is sent through a frequency divider to further cut the frequency in half. It's possible to repeat the procedure until the target frequency or range is achieved [8].

The mobile market is still expanding and growing at rapid pace. Wearable information equipment especially that related to healthcare has seen a recent boom in development alongside more traditional mobile phones, digital cameras, and tablets [9]. The demand for power reduction in VLSI is rising, making it a more relevant problem in battery operated devices. On the basis of this foundation, several circuit techniques have been presented [10]–[15]. About half of the power dissipation in VLSI is attributable to random logic, with flip-flops accounting for about a third of that total. In the last decade, various low-power FFs have been hastily developed. However, the traditional FF is still the most popular choice for real chip design due to its optimal mix of performance, power, and cell area. This paper's objective is to offer a frequency divider circuit employing a flip-flop that does not compromise on performance in either timing or cell size while still reducing PDP. The proposed flip-flop for the frequency divider is a sense amplifier based flip flop.

2 Proposed frequency divider using sense amplifier based FF

2.1 Frequency divider circuit

Different components of digital systems often need tens or hundreds of clock signals. In a field programmable gate array (FPGA) based system, for instance, a 48 kHz

clock may be used to generate an audio stream, a 1 kHz clock could power a timer, a 10 MHz clock could power a microprocessor, and a 12 kHz clock could power a motor controller. Since it would be exorbitantly expensive to employ many external oscillator circuits to generate the various clock signals required by a system, most of these signals are generated internally from a single or dual master clock input.

A clock divider circuit generates clock signals at a lower frequency from a higher frequency clock source. The divider circuit counts the number of clock cycles on the input side and sends low and high signals to the output clock at different times. One D-type FF logic element is used in the circuit's division by two operation. The output Q may be obtained by simply feeding the pulse train into the clock circuit and connecting the complement output QB to the input D as shown in Figure 1 for a 3-bit divider. The circuit has a straightforward operation. The incoming pulse train, which carries the data from the D input to the output, times the device, the subsequent stages divides it to half. The core part of this frequency divider is the D-type FF.

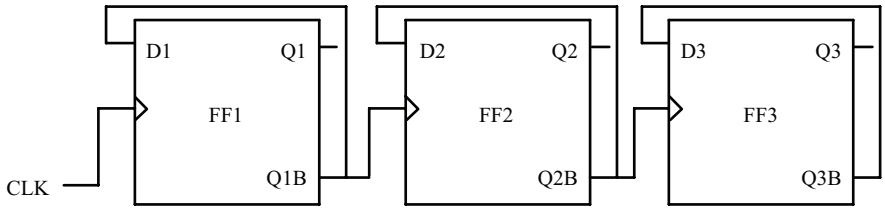


Fig. 1. Circuit configuration of 3-bit frequency divider

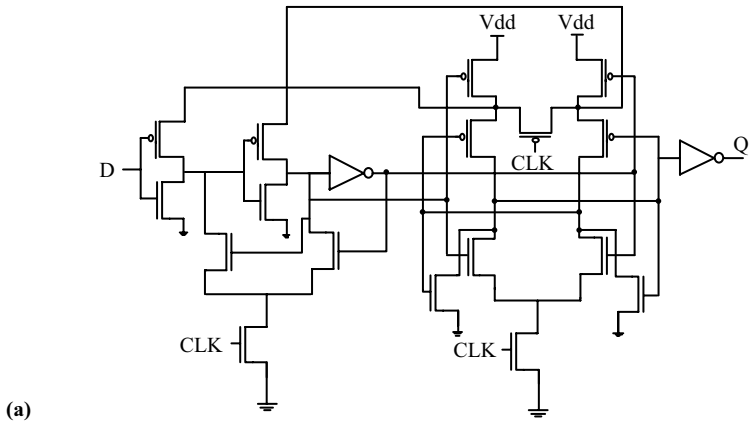
2.2 Investigated FFs

Four existing D-type FF are investigated in this section. Figure 2a proposed by [16] known as Topologically Compressed FF (TCFF) has only three transistors directly involved with the timekeeping. The omission of a pre-charge circuit or a dynamic circuit means that no additional power is being wasted. This strategy for shrinking data is what is termed the Topological Compression approach. When the clock signal (CLK) is low, the TCFF is formed by activating the PMOS transistor connected to CLK. This causes the master latch to activate the data input mode. The data from D's input is saved in the master latch. When CLK is high, the slave latch switches to data output mode, turning ON the NMOS linked to CLK and turning OFF the PMOS transistor attached to CLK. Under these circumstances, the contents of the master latch are copied into the slave latch and sent on to the output. All terminals are at rest and in full swing throughout this procedure. Since the master and slave latch take turns being functional, the current that comes from the power source does not flow into both of them at the same time. This prevents a conflict in the operation of the latches. Due to the modest impact of timing deterioration on cell performance, numerous transistors may be shared without increasing transistor size.

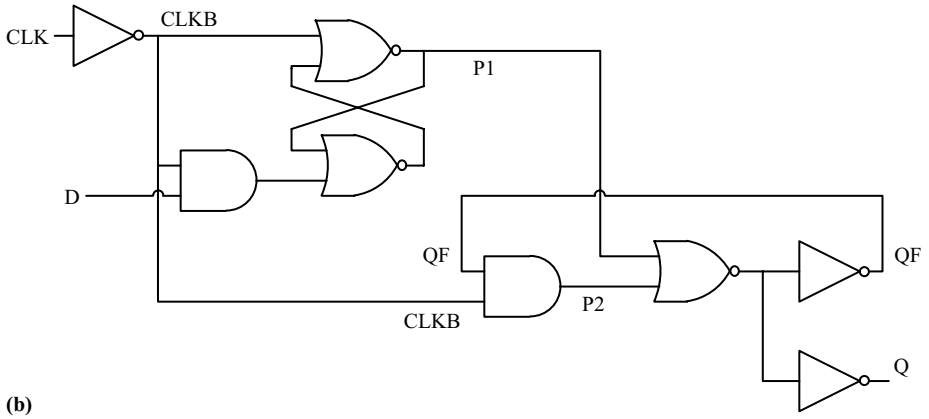
Rasouli in [17] proposed a semi-self-gated flip-flop shown in Figure 2b. The slave latch AND gate outputs a zero to the one input of the slave latch NOR gate when the

clock signal is a one (i.e. CLK=1). Latch NOR gate therefore inverts the output of the master latch circuit. The output Q is created by the slave latch inverter. Since the slave latch NOR gate acts as an inverter when CLK=0, its output may be used to supplement the signal from the slave latch AND gate when CLKB is high. Therefore, the optimum coupling between the inverter's output QF and the slave latch NOR gate is established. Instead of producing a series of discrete pulses whenever the input data changes, node P2 creates a controlled input clock train, which activates the clock signal at input high values and deactivates it at low values. This means the flip flop is only partially self-gated, earning it the name "semi-gated."

Nikolic's in [18] proposed a novel symmetric arrangement for the latch stage, as depicted in Figure 2c. To get this layout, k-map was used for logical reduction, and the resulting structure is an AND-OR topology. These characteristics are reflected in the resulting latch.

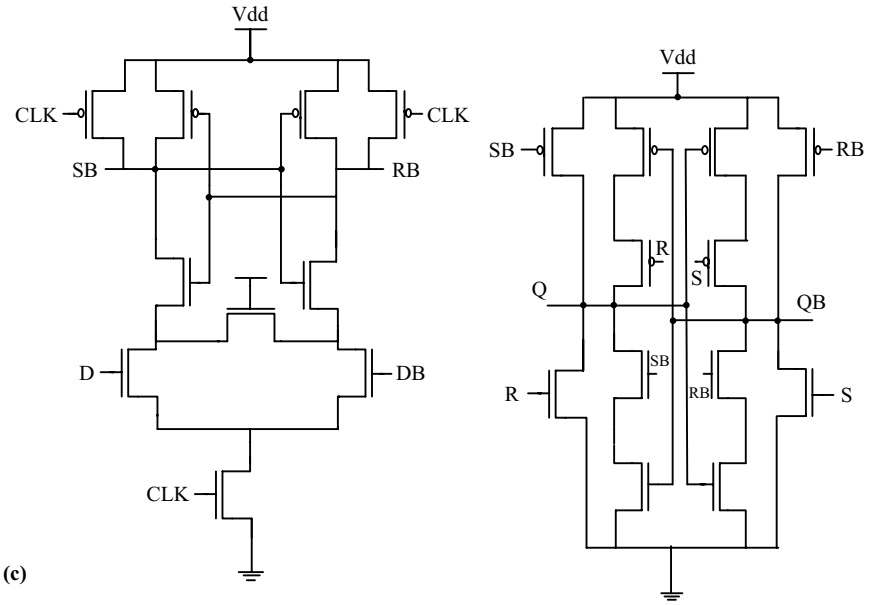


(a)

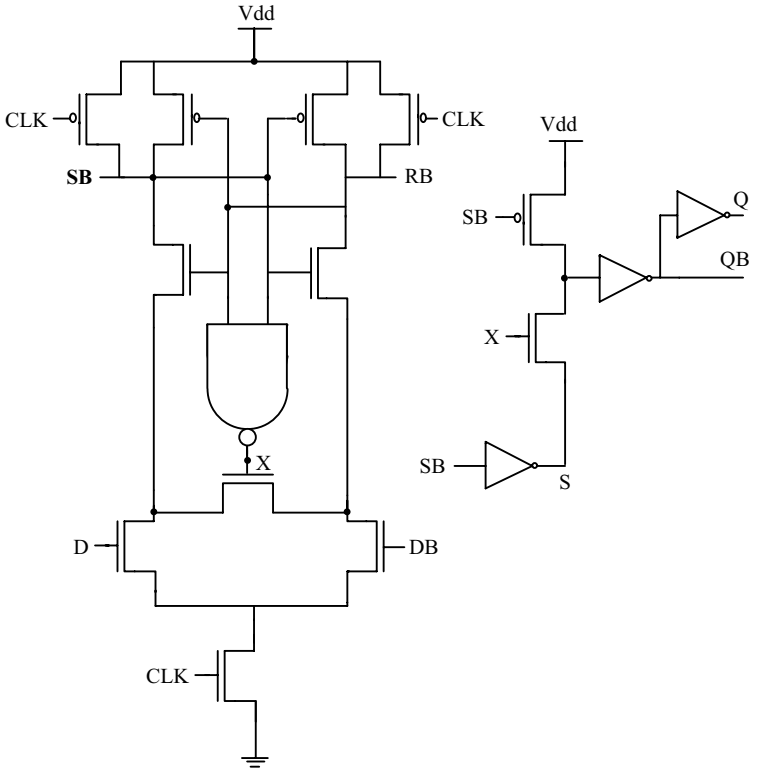


(b)

Fig. 2. *(Continued)*



(c)



(d)

Fig. 2. Conventional FF designs (a) TCFF [16] (b) Rasouli's FF [17] (c) Nikolic's FF [18] (d) Shah's FF [19]

The tiny size of the keeper transistors is made possible by the fact that just a single transistor in each branch is active during the state change and that the delays at the normal and complement nodes are the same. Not only are these advantages gained, but power consumption is also lowered by maintaining a single active transistor between transitions. When employed in CMOS circuit design, the flip flop's effectiveness is essentially doubled due to the symmetry between its two outputs, both of which have the same driving strength.

Figure 2d proposed by [19] is a version of a single-ended sense amplifier flip-flop that relies on a detection signal derived from the sensing stage's outputs using a two-input NAND gate. When the clock is low, the sensing stage of the sense amplifier flip flop precharges both SB and RB to high, resulting in a low signal at the NAND gate's output. The sensing stage transition now begins when the clock goes high, and when it's finished, either SB or RB, depending on the data in D, will be in their low states. The NAND gate's output becomes high at this moment. Because this NAND gate's output signal is coupled to transistor NMOS gate terminal disabling it during the transition and enabling afterwards. In contrast to earlier sense amplifiers, when this transistor were always ON, the sensing stage's speed is unaffected by the lower supply voltages. The detection signal created in the sensing stage is used in place of the global clock in the latching stage.

2.3 Proposed SAFF

After evaluating the strengths and limitations of previous FF designs in depth, a new sense amplifier based FF is proposed in Figure 3. This SAFF uses the same sensing stage as was used by [18]. The latching stage is a single-ended structure and due to its single-ended design, the latching stage doesn't accept the signal SB as an input and only RB is used. To illustrate how the flip flop works, consider what happens if input signal data D is high: during the rising edges of the clock, RB will stay at operating voltage (Vdd), and node C will be discharged to low through transistor N7. Now node RB discharges to low in response to a low value at the input data D, transistor P5 turns ON. Transistors P5 and N7 are now pulling node C to Vdd. The outputs QB and Q are driven by two inverters that are coupled at node C. This proposed FF architecture has both the true and compliment output available as is required for frequency dividers.

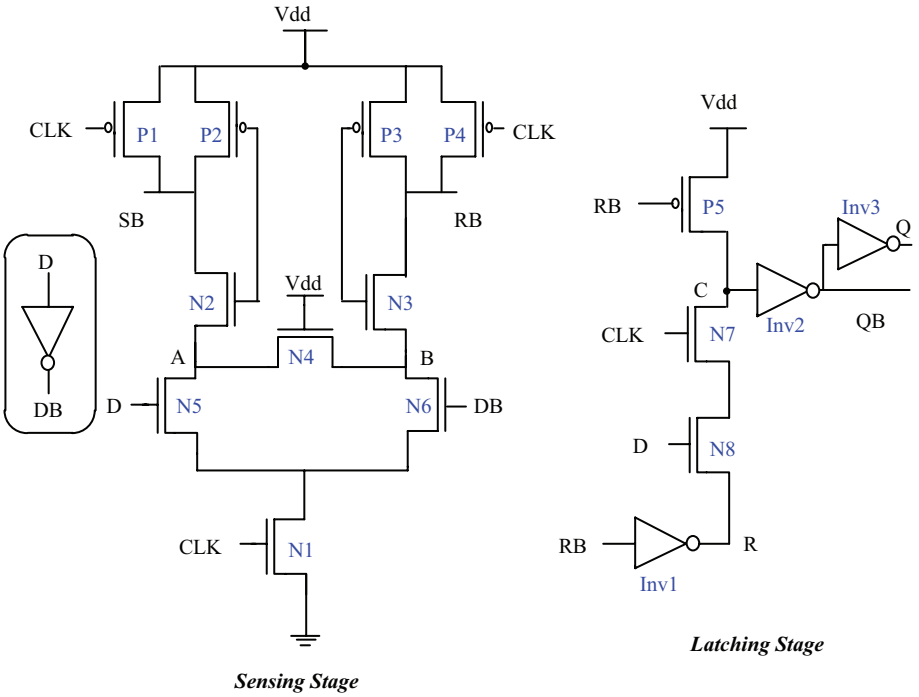


Fig. 3. Architecture of proposed FF

2.4 Proposed 3-bit frequency divider

The FFs discussed in preceding sections along with the proposed FF are used to implement a 3-bit frequency divider. Figure 4 shows the circuit diagram of 3-bit frequency divider using the proposed FF. The transient waveform of this frequency divider is shown in Figure 5. It is important to pay attention to what occurs at each step of the waveforms that are shown in Figure 5 if one wants to have a comprehensive understanding of the functioning of the circuit. Consider the case when Q1 is returning a value of "1". This results in a value of "0" being generated from the output Q1B. On the next rising edge of the clock input pulse train, this information is sent on to the output Q1. At this point, the output changes from a one to a zero. Once again, information from the Q1B output is clocked through at the next positive clock pulse. Since it is now a '1' (the opposite of the Q1 output), it is passed on, and the output goes through yet another state transition. It is evident that the circuit's output only transitions between states on the rising and falling edges of the incoming pulse clock signal. Given that the D-type circuit's output needs two transitions to complete a cycle, the frequency of transitions in the D-type circuit is exactly half that of the incoming pulse train, even if each positive edge occurs once per cycle. That is to say, it has been cut in half.

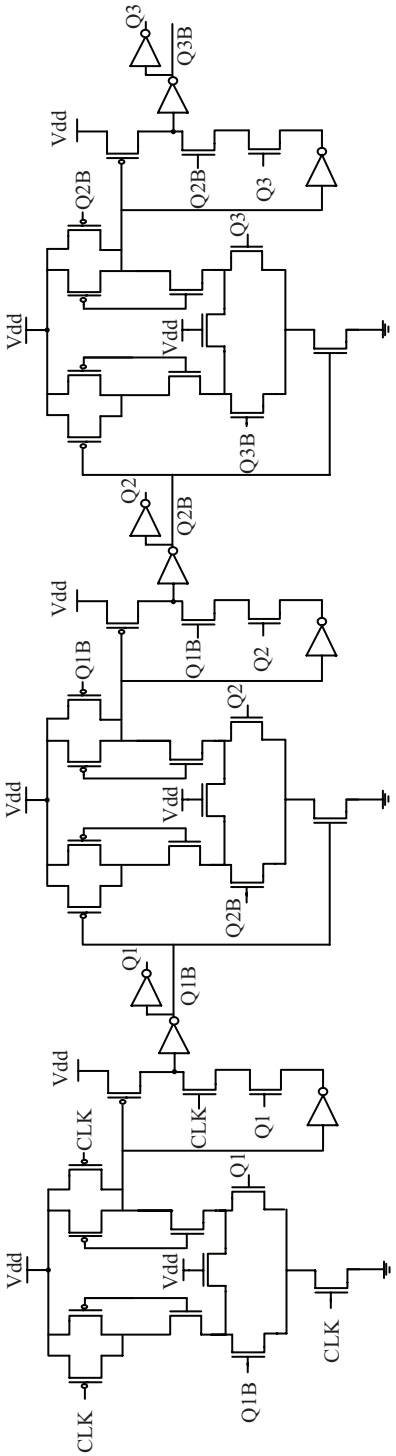


Fig. 4. Proposed 3-bit frequency divider

When working with this kind of circuit, there are a few safety measures that should be taken. The primary one is that the pulse train must have crisp discontinuities. Inadequately sharp rising edges may cause the circuit to malfunction. If this is the case, connecting an inverter to the clock input may be the solution to the problem. Keep in mind that the flip-flops in FPGAs (like the chip on-board) can only be clocked by the main clock input or by the output of another flip-flop. Therefore in order to generate another cut in half frequency, subsequent FF stage is to be added the input of which is connected to the output of previous stage. As in for a 3-bit frequency divider, three such FFs need to be arranged as shown in Figure 4. A clock with a frequency of 1 kHz may be generated by the circuit by dividing the primary clock (CLK), which has an input frequency of 100 MHz, by 100,000. The output Q1, Q2 and Q3 in Figure 5 shows the 3-stage division in frequency.

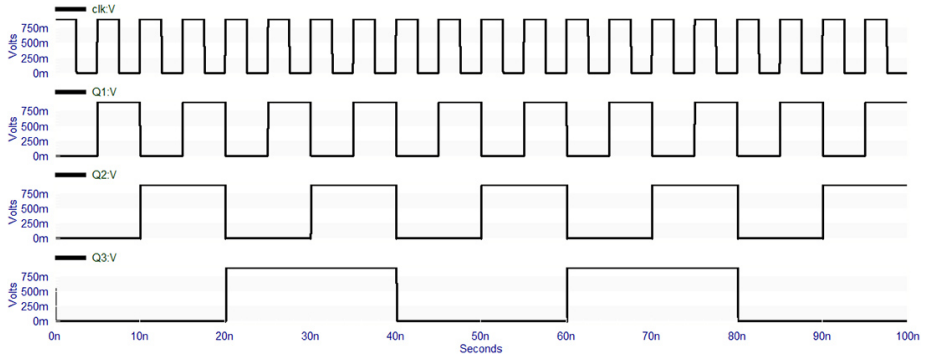
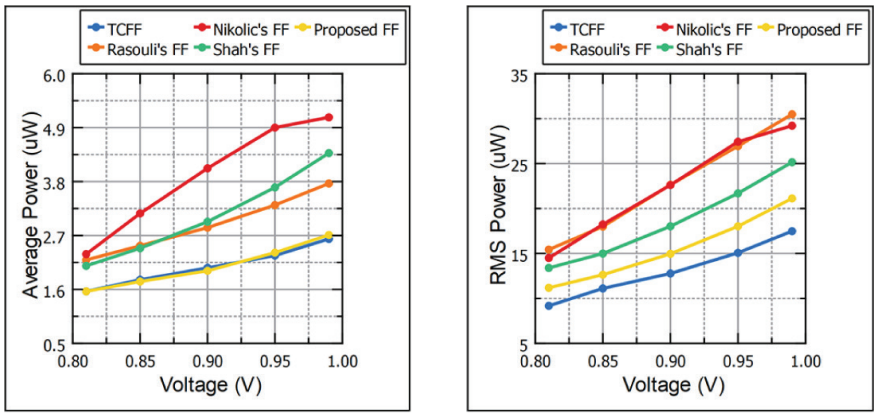


Fig. 5. Operational waveform of proposed 3-bit frequency divider

3 Simulation results & discussions

To show the advantages of the proposed frequency divider design, post-layout simulations were performed with available designs to determine the performance characteristics. The designs include the four architectures depicted in Figure 2 (TCFF, Rasouli's FF, Nikolic's FF and Shah's FF). The CMOS process developed by [20] at 32 nanometers has been chosen as the target technology. The nominal operating conditions are 200 MHz/0.9 V at 25 °C temperature. Each design is improved by considering the transistor size tweaking. Post-layout parasitic extraction and subsequent measurements are performed under varying Process, Voltage and Temperature (PVT) settings.

In order to calculate the power used by the FDs and to investigate the behavior of the FD designs under consideration for variation in voltage, five different voltages are applied (at 10% variance to supply voltage). These findings regarding the power consumption which includes both the average power and RMS power is shown in Figure 6.



(a) **(b)**

Fig. 6. Power consumption at variations in voltage (a) average power (b) RMS power

Table 1 shows the speed of operation of various FDs at voltage variation of ±10% to nominal voltage. This test was performed using the global clock CLK as reference and observations were taken at all FF outputs (Q1, Q2 and Q3) of the FD. Nearly at all observed parameters, the proposed FD was fastest compared to its counterparts. Timing parameters are the true measurements of FD's performance, with power delay product (PDP) being the most crucial metric.

Table 1. Three stage clock to output delay at variations in voltage

Flip Flop Used		TCFF	Rasouli's FF	Nikolic's FF	Shah's FF	Proposed FF
CLK-Q1 delay (ps)	@0.81 V	35.03	43.33	32.66	43.33	30.3
	@0.85 V	32.48	38.37	29.53	39.51	22.88
	@0.9 V	30.38	34.69	23.89	35.58	22.76
	@0.95 V	29.44	32.82	21.04	32.87	20.3
	@0.99 V	28.4	31.45	19.17	31.39	18.9
CLK-Q2 delay (ps)	@0.81 V	80.37	87.54	77.11	87.29	70.79
	@0.85 V	75.31	78.22	69.65	79.7	61.77
	@0.9 V	65.44	65.25	60.71	71.134	56.87
	@0.95 V	58.98	65.02	54.8	65.066	50.92
	@0.99 V	55.43	59.53	50.52	61.4	47.65
CLK-Q3 delay (ps)	@0.81 V	125.76	133.71	112.94	128.52	110.1
	@0.85 V	115.54	119.61	105.24	116.1	104.65
	@0.9 V	101.96	102.62	93.54	103.17	93.92
	@0.95 V	89.02	99.15	88.54	92.29	84.22
	@0.81 V	35.03	43.33	32.66	43.33	30.3

Figure 7 shows the PDP performance of all FDs at different voltage levels. Taken into consideration here is also the intermediate stage PDP i.e. the PDP from CLK-Q1, Q1–Q2 and Q2–Q3 as these parameters are of most importance in any FD design.

Based on the findings, the proposed FD had the lowest PDP of the bunch. In comparison to TCFF, Rasouli's FF, Nikolic's FF and Shah's FF respectively, at nominal operating conditions, it reduces overall PDP by 27.28%, 54.57%, 53.65% and 57.49% while maintaining better speed performance.

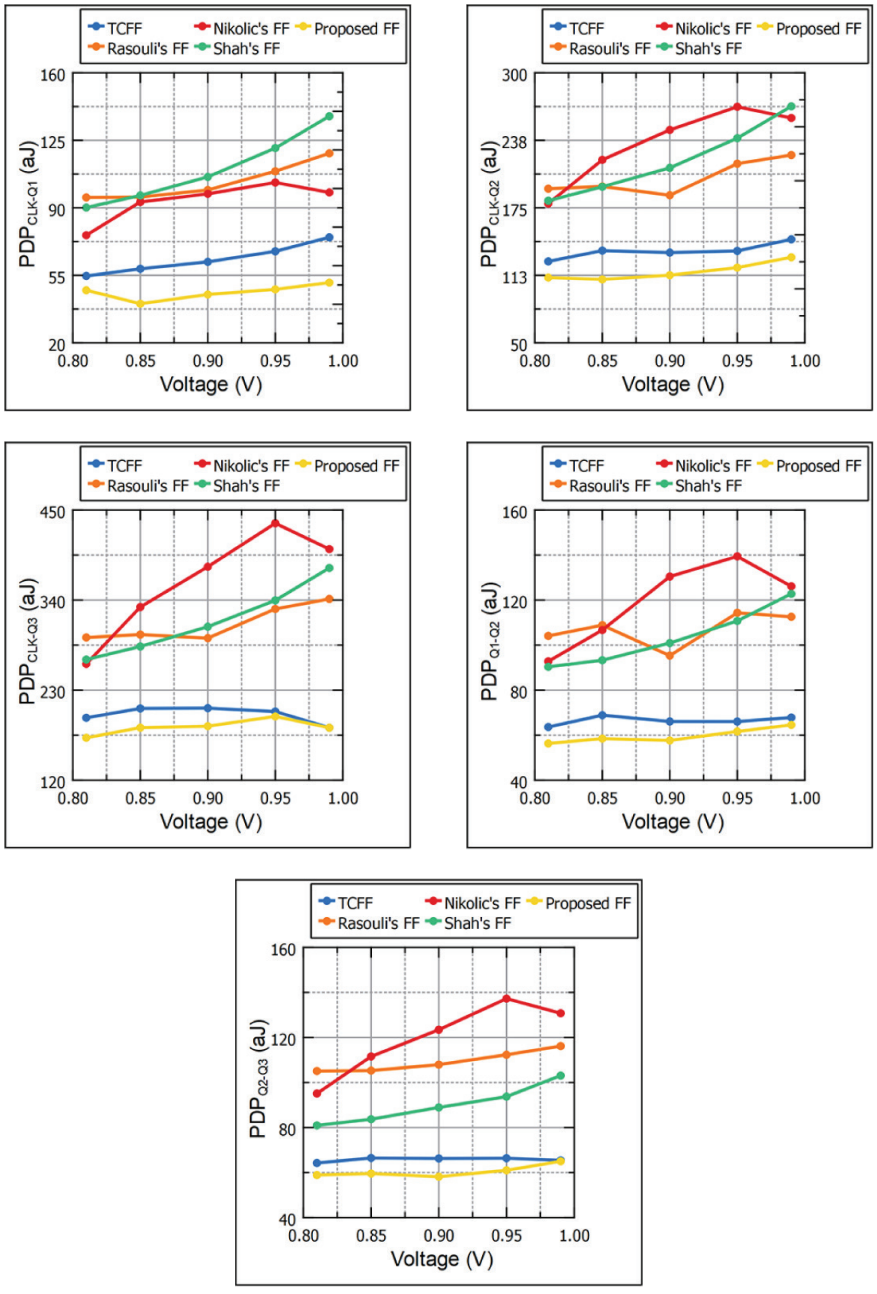
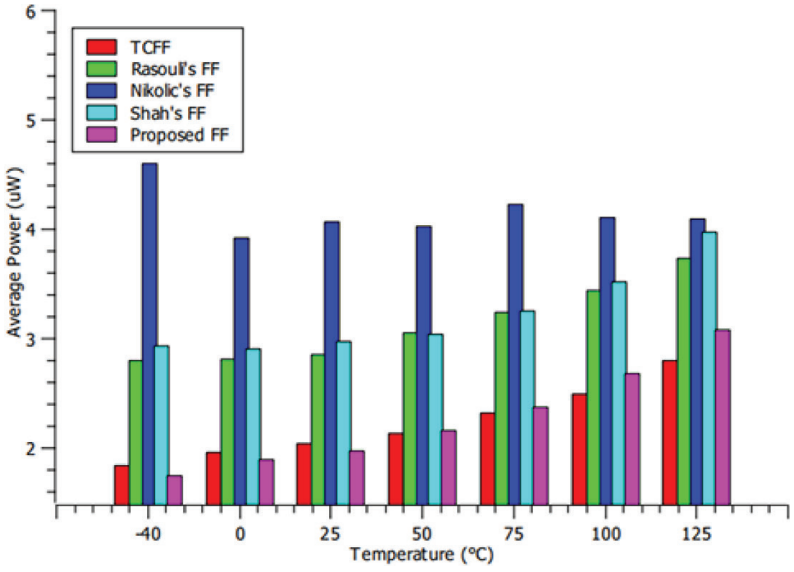
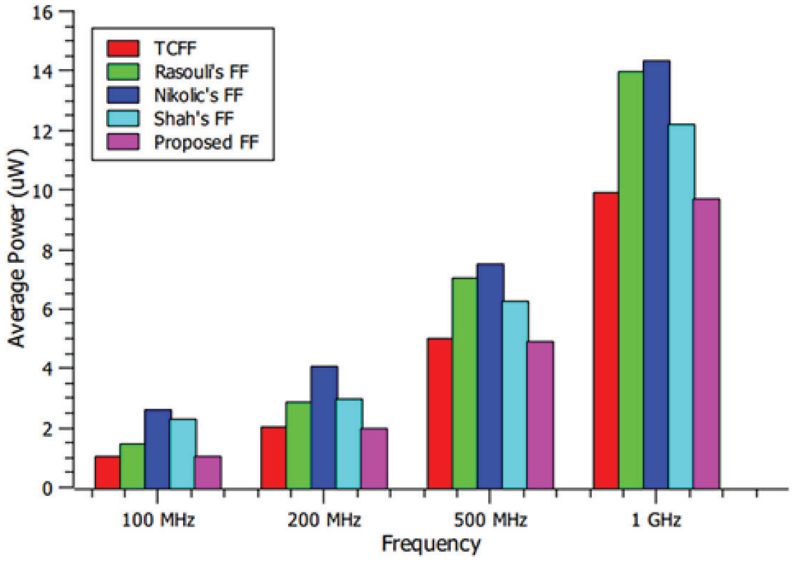


Fig. 7. PDP performance at different voltages

Figure 8 displays the power results under two circumstances that are used to further examine the design enhancements: the temperature, and the frequency. Wide range of temperature varying from minimum −40 °C to maximum 125 °C was tested. Further the power calculations were taken at four different frequencies of 100 MHz, 200 MHz, 500 MHz and 1 GHz. In both tests proposed FD offered power performance that is at par with TCFF and better than that of other FDs compared.



(a)



(b)

Fig. 8. Average power at variations in (a) temperature (b) frequency

Table 2 displays the intermediate stage delay at variations in aforementioned temperature range. The proposed FD has a shorter delay period for all stage delays and for all variations in temperature.

Table 2. Intermediate stage delay at variations in temperature

Flip Flop Used		TCFF	Rasouli's FF	Nikolic's FF	Shah's FF	Proposed FF
CLK-Q1 delay (ps)	@−40°C	21.85	25.75	19.11	24.72	17.7
	@0°C	27.59	29.69	23.63	30.2	21.22
	@25°C	30.38	34.69	23.89	35.58	22.76
	@50°C	34.48	40.42	25.17	40.82	24.72
	@75°C	38.6	46.84	30.16	47.29	26.37
	@100°C	42.53	52.81	34.1	54.32	30.52
	@125°C	46.81	59.51	38.33	59.34	34.2
Q1–Q2 delay (ps)	@−40°C	21.34	24.86	20.61	22.91	18.15
	@0°C	28.22	24.18	27.57	29.53	25.55
	@25°C	32.39	33.33	32.05	33.86	29.12
	@50°C	39.04	44.55	36.08	38.93	34.98
	@75°C	43.7	51.05	41.92	44.44	37.59
	@100°C	50.46	59.01	48.52	49.1	44.94
	@125°C	56.44	67.26	55.51	56.15	50.533
Q2–Q3 delay (ps)	@−40°C	22.57	24.44	22.12	20.34	19.64
	@0°C	28.15	31.84	26.02	25.68	25.89
	@25°C	32.49	37.74	30.33	29.84	29.38
	@50°C	38.05	44.25	35.31	34.186	33.66
	@75°C	43.37	50.84	40.78	39.27	38.35
	@100°C	50.31	59.308	47.51	43.78	43.56
	@125°C	56.45	66.37	53.61	49.37	47.65

Figure 9 shows how the proposed FD compares to other designs in terms of PDP at a wide range of temperatures. It is important to point out that the intermediate stage PDP performance of the Nikolic's design at temperatures less than 75 °C is the worst compared to that of other designs since the average power of this design is so significant.

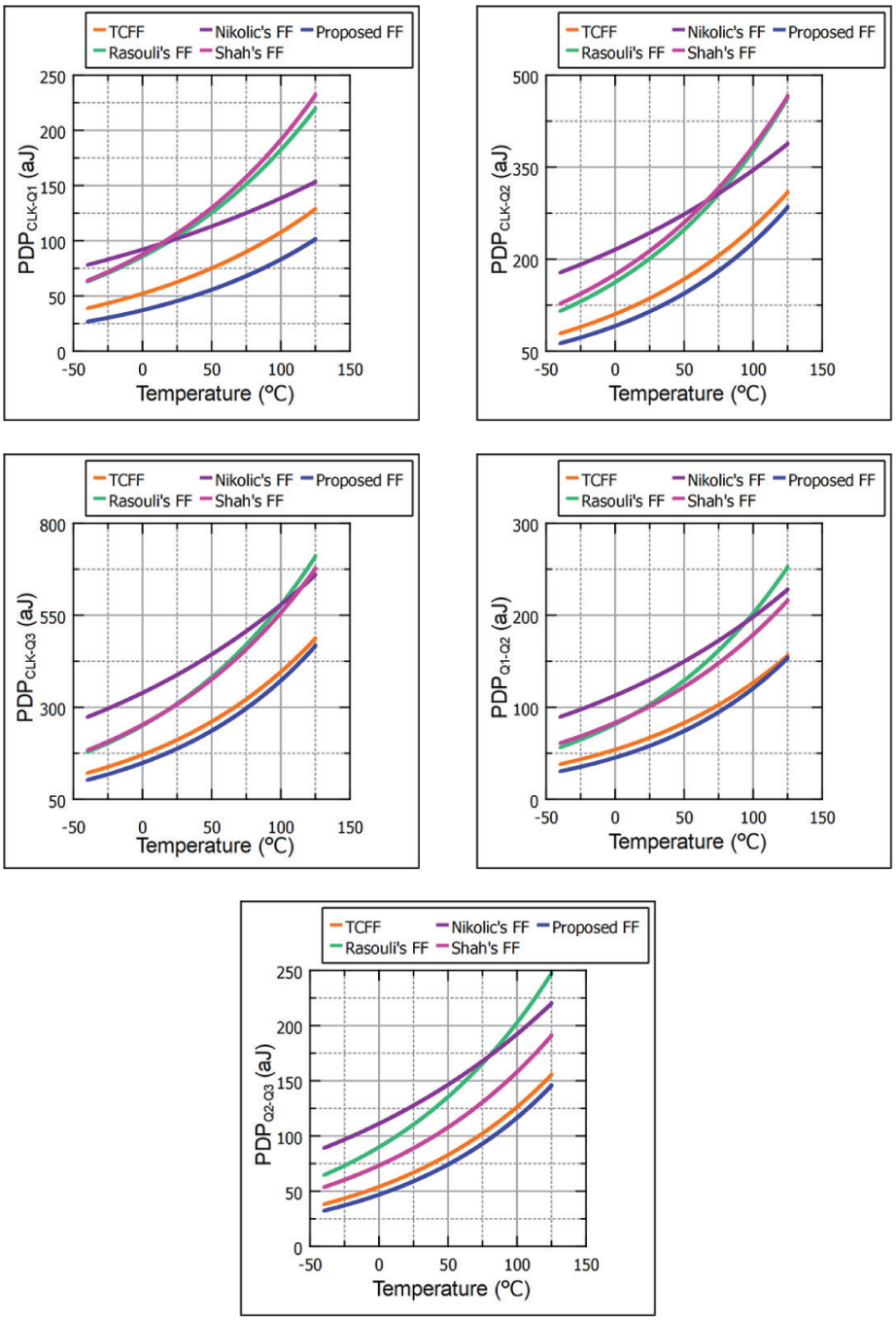


Fig. 9. PDP performance at different temperatures

In terms of area overhead, the proposed FD has least transistor count of '63' followed by FD using TCFF with '69' and Shah's FF at '72'. Rasouli's design has maximum transistor count of '96'. It is worth mentioning here that the total layout area when sum of widths (W) is taken into account of the proposed FD is at par with TCFF FD whereas Nikolic's design requires maximum area among all designs. These area requirements can be seen and is presented in Figure 10.

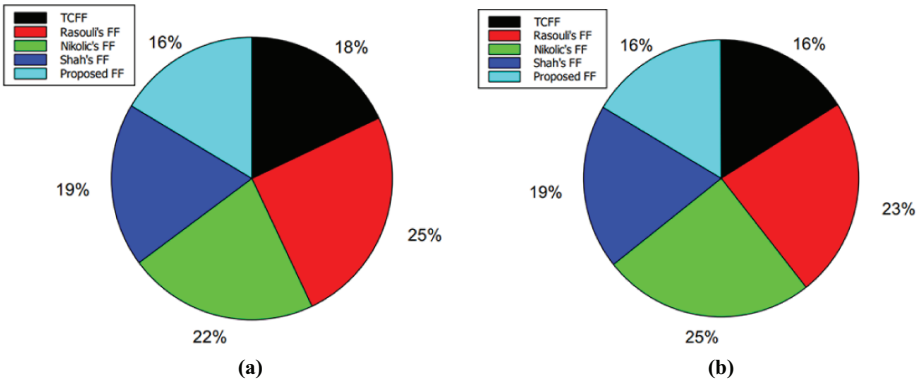


Fig. 10. Area comparison of different frequency dividers (a) no. of transistors (b) layout area (in μm^2)

Table 3 depicts the power performance at various process corners. This performance is achieved under the following circumstances, each of which is used as a distinct process corner: SS = 0.8 V/125 °C, FF = 1 V/ −40 °C, TT = 0.9 V/25 °C, FS = 0.9 V/25 °C and SF = 0.9 V/25 °C.

Table 3. Average power (μW) at different process corners

Frequency Divider	FF	FS	TT	SF	SS
TCFF	2.77	2.607	2.04	1.832	2.091
Rasouli's FF	3.96	3.64	2.86	2.64	2.81
Nikolic's FF	4.99	5.68	4.07	3.66	3.89
Shah's FF	3.58	4.61	2.98	2.53	2.55
Proposed FF	2.93	3.07	1.98	1.82	2.01

The comparisons in Table 3 demonstrate that the proposed FD's power results are at par with TCFF at corner cases of TT, SF and SS whereas the scenarios in which the proposed architecture performs less well than TCFF is at FF and FS corner.

Additionally, due to the fast operating speed, the corner case PDP findings of the proposed FD have shown an improvement over available designs as can be seen in Figure 11. In contrast, the PDP performance of the Nikolic's design at intermediate stage of Q1–Q2 and Q2–Q3 is the worst of any other design when measured in various process corners.

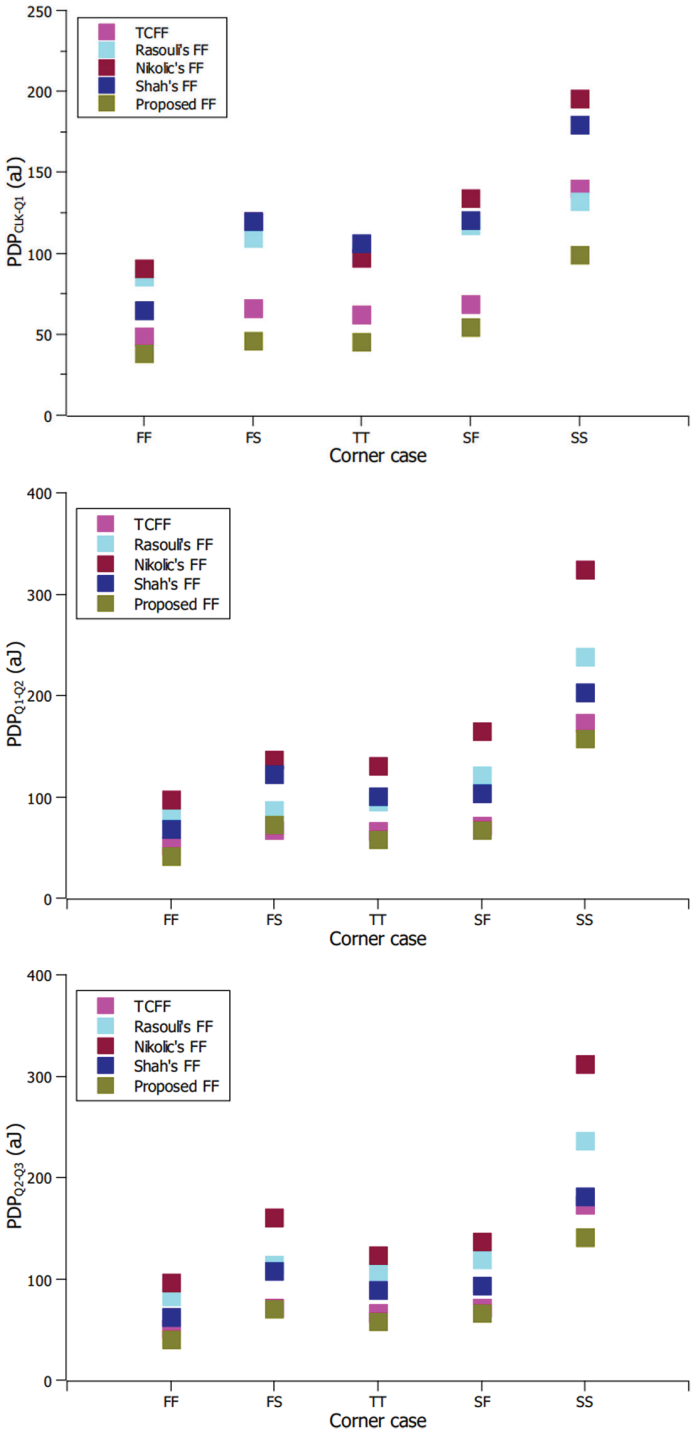


Fig. 11. PDP performance for corner cases

In addition to the findings presented above, the proposed FD was further tested for up to 5-bits (five divisions), the result of which showcases the worthiness of the design as is shown in Figure 12.

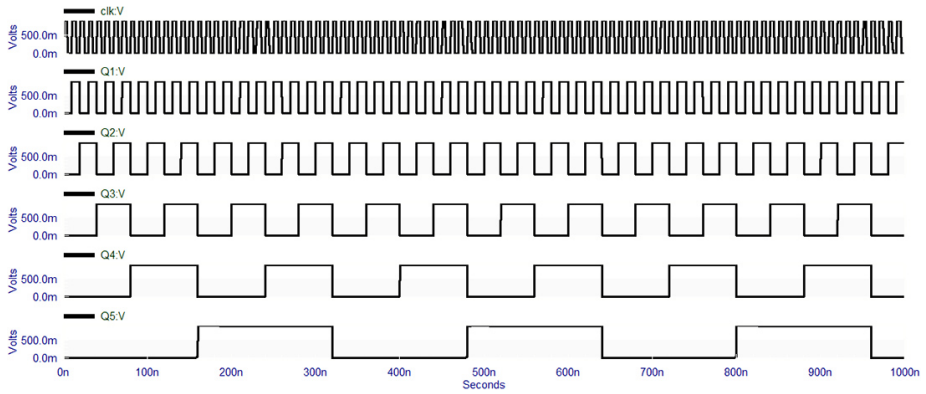


Fig. 12. Test result of 5-bit frequency divider

4 Conclusions

In this study, a new design for a flip-flop is proposed that improves the efficiency of power delay product for its use in memory cells and processors. The proposed flip-flop was used as a 3-bit frequency divider. The simulation results highlight the advantageous qualities of the proposed design in comparison to those of alternative options. The delay time for switching was substantially decreased which resulted in better PDP values at wide voltage, temperature and frequency variations. The proposed design is also area efficient and utilizes area similar to that of TCFF.

5 References

[1] H. You, J. Yuan, W. Tang, Z. Yu, and S. Qiao, "A Low-Power High-Speed Sense-Amplifier-Based Flip-Flop in 55 nm MTCMOS," Electronics, vol. 9, no. 5, p. 802, May 2020. https://doi.org/10.3390/electronics9050802

[2] O. A. Shah, I. Ahmed Khan, G. Nijhawan, and I. Garg, "Low Transistor Count Storage Elements and their Performance Comparison," in 2018 International Conference on Advances in Computing, Communication Control and Networking (ICACCCN), Greater Noida (UP), India, Oct. 2018, pp. 801–805. https://doi.org/10.1109/ICACCCN.2018.8748364

[3] H. Zhuang, C. Tong, X. Peng, and H. Tang, "Low-Power, Low-Noise Edge-Race Comparator for SAR ADCs," IEEE Trans. VLSI Syst., vol. 28, no. 12, pp. 2699–2707, Dec. 2020. https://doi.org/10.1109/TVLSI.2020.3021680

[4] N. T. Tasneem, S. A. Pullano, C. D. Critello, A. S. Fiorillo, and I. Mahbub, "A Low-Power On-Chip ECG Monitoring System Based on MWCNT/PDMS Dry Electrodes," IEEE Sensors J., vol. 20, no. 21, pp. 12799–12806, Nov. 2020. https://doi.org/10.1109/JSEN.2020.3001209

[5] K. P. Ayodele, W. O. Ikezogwo, and A. A. Osuntuyi, "Empirical Characterization of the Temporal Dynamics of EEG Spectral Components," Int. J. Onl. Eng., vol. 16, no. 15, p. 80, Dec. 2020. https://doi.org/10.3991/ijoe.v16i15.16663

[6] H. K. Aljobouri, "A Virtual EMG Signal Control and Analysis for Optimal Hardware Design," Int. J. Onl. Eng., vol. 18, no. 02, pp. 154–166, Feb. 2022. https://doi.org/10.3991/ijoe.v18i02.27047

[7] D.-S. Lee et al., "A Wide-Locking-Range Dual Injection-Locked Frequency Divider with An Automatic Frequency Calibration Loop in 65-nm CMOS," IEEE Trans. Circuits Syst. II, vol. 62, no. 4, pp. 327–331, Apr. 2015. https://doi.org/10.1109/TCSII.2014.2387591

[8] S. Agarwal, A. Pathy, and Z. Abbas, "A 9.5nW, 0.55V Supply, CMOS Current Reference for Low Power Biomedical Applications," IEEE Trans. Circuits Syst. II, vol. 69, no. 9, pp. 3650–3654, Sep. 2022. https://doi.org/10.1109/TCSII.2022.3183146

[9] F. Hu, Y. Xiao, and Q. Hao, "Congestion-Aware, Loss-Resilient Bio-Monitoring Sensor Networking for Mobile Health Applications," IEEE J. Select. Areas Commun., vol. 27, no. 4, pp. 450–465, May 2009. https://doi.org/10.1109/JSAC.2009.090509

[10] H. Bhamra, Y.-W. Huang, Q. Yuan, and P. Irazoqui, "An Ultra-Low Power 2.4 GHz Transmitter for Energy Harvested Wireless Sensor Nodes and Biomedical Devices," IEEE Trans. Circuits Syst. II, vol. 68, no. 1, pp. 206–210, Jan. 2021. https://doi.org/10.1109/TCSII.2020.3005332

[11] H. Wang, Y. Li, and J. Wang, "A Novel Power Saving Algorithm for Wireless Sensor Networks," Int. J. Onl. Eng., vol. 9, no. 5, p. 78, Sep. 2013. https://doi.org/10.3991/ijoe.v9i5.2977

[12] I. A. Khan, O. A. Shah, and M. T. Beg, "Analysis of different techniques for low power Single Edge Triggered Flip Flops," in 2011 World Congress on Information and Communication Technologies, Mumbai, India, Dec. 2011, pp. 1363–1367. https://doi.org/10.1109/WICT.2011.6141447

[13] B. Yazdani and S. Jafarabadi Ashtiani, "A Low Power Fully Differential Level-Crossing ADC with Low Power Charge Redistribution Input for Biomedical Applications," IEEE Trans. Circuits Syst. II, vol. 69, no. 3, pp. 864–868, Mar. 2022. https://doi.org/10.1109/TCSII.2021.3127279

[14] Z. Liu, Y. Tan, H. Li, H. Jiang, J. Liu, and H. Liao, "A 0.5-V 3.69-nW Complementary Source-Follower-C Based Low-Pass Filter for Wearable Biomedical Applications," IEEE Trans. Circuits Syst. I, vol. 67, no. 12, pp. 4370–4381, Dec. 2020. https://doi.org/10.1109/TCSI.2020.2995351

[15] O. A. Shah, G. Nijhawan, and I. A. Khan, "Low Power Area Efficient Self-Gated Flip Flop: Design, Implementation and Analysis in Emerging Devices," Engineering and Applied Science Research, vol. 49, no. 6, pp. 744–752, 2022. https://doi.org/10.14456/EASR.2022.72.

[16] N. Kawai et al., "A Fully Static Topologically-Compressed 21-Transistor Flip-Flop with 75% Power Saving," IEEE J. Solid-State Circuits, vol. 49, no. 11, pp. 2526–2533, Nov. 2014. https://doi.org/10.1109/JSSC.2014.2332532

[17] S. H. Rasouli, X. Chen, and V. Boynapalli, "Semi-Data Gated Flop with Low Clock Power/Low Internal Power with Minimal Area Overhead," US 9, 979, 381 B1, May 22, 2018.

[18] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, Wenyan Jia, James Kar-Shing Chiu, and M. Ming-Tak Leung, "Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements," IEEE J. Solid-State Circuits, vol. 35, no. 6, pp. 876–884, Jun. 2000. https://doi.org/10.1109/4.845191

[19] O. A. Shah, G. Nijhawan, and I. A. Khan, "Improved Sense Amplifier Based Flip Flop Design for Low Power and High Data Activity Circuits," Journal of Applied Science and Engineering, vol. 26, no. 7, pp. 1047–1053, Oct. 2022. https://doi.org/10.6180/jase.202307_26(7).0015.

[20] "Predictive Technology Model," PTM, 2012. https://ptm.asu.edu (accessed Oct. 10, 2022).

6 Authors

Sanjay Grewal obtained B.Tech. degree in Electronics & Communication Engineering from Uttar Pradesh Technical University, Lucknow, India. He is currently working towards his Masters of Technology degree in Information & Communication Technology from Noida International University. His research interest involves low power design and applications of technologies in the medical field.

Owais Ahmad Shah holds a Doctorate degree in Engineering with specialization in low power design. He obtained his Masters of Technology degree in VLSI Design from Uttar Pradesh Technical University, Lucknow, India. Prior to that, he earned a Bachelor's degree in Electronics & Communication Engineering from the same university. His research interests include synchronous VLSI designs, low-power VLSI circuit designs, and low-voltage embedded memory circuit designs. His commitment to exploring novel approaches to VLSI designs and low-power circuitry makes him a valuable asset in the pursuit of more efficient and sustainable electronic devices. Through his expertise and ongoing research endeavors, he seeks to advance the state-of-the-art in VLSI design, contributing to the development of energy-efficient and high-performance electronic systems.

Article submitted 2023-02-24. Resubmitted 2023-03-27. Final acceptance 2023-04-01. Final version published as submitted by the authors.