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PAPER

# A Case for Low-Cost Personal Electronic Laboratory Equipment Using FPGAs

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**ABSTRACT**

The field of reconfigurable computing is gaining a lot of following, and several use cases have been developed for it. At the centre of reconfigurable computing is the field programmable gate array (FPGA) due to its computational speed and versatility. The goal of the work reported here was to show that a single FPGA board paired with a computer monitor can be used as the sole laboratory equipment in a cash-strapped educational institution or by an individual. A Terasic DE1-SoC board was programmed as an oscilloscope, and digital multimeter. In keeping with the low-cost theme of this work, no external signal conditioning circuit was used and the on-board LTC2308 ADC was used for signal acquisition. At frequencies below 15 kHz, the voltage measurements of the developed FPGA lab instrument had a mean error of 58 mV. The voltage measurement errors, however, increased with an increase in frequency and the errors were significant when the signal frequencies exceeded 100 kHz. In terms of the use of the FPGA to replace multiple lab instruments, 13% of the DSPs on the FPGA were used for the implementation and 80% of the Adaptive logic modules. We therefore demonstrate that with $300 dollars, multiple pieces of laboratory equipment can be replaced by a single FPGA board and a monitor.

**KEYWORDS**

FPGA, reconfigurable hardware, low cost, laboratory, programmable

## 1 INTRODUCTION

Laboratory education is an essential requirement for an engineering education [1], [2]. A laboratory is itself a tool where theoretical concepts and principles can be experimented on to validate them, demonstrate them, extend them, and query them. The phrase "learn by doing" is the foundation of laboratory education. Thus, it is very essential for every engineering student to have time to perform experiments. This raises the question of how to make it feasible to provide laboratory education to each engineering student in each institution.

In the home country of the authors, most of the public universities are unable to provide or accommodate individual experiment set-ups for their electronic/electrical

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engineering (EEE) students during laboratory sessions. The main reason cited is the cost. There are two costs involved here: the cost of laboratory space and the cost of equipment. The former refers to the fact that there often are no sufficiently large laboratory spaces that can accommodate individual experimental set-ups for each student. This paper does not address this challenge, but it does address the latter problem: the cost of equipment. Several EEE laboratories (the authors visited four universities in their country and had informal interactions with staff of several others) site the lack of sufficient equipment due to poor/insufficient funding. This study was fuelled by this need.

Some of the most basic instruments used in most EEE laboratories include oscilloscopes, function generators, spectrum analysers, logic analysers, and multimeters. This list of five instruments, if one is purchasing the conventional traditional instruments, conservatively cost about $2,000 on the market at present. This cost is unfortunately high for poorly funded institutions. It is for this reason that recent years have seen the introduction of low-cost laboratory instruments [3] such as the National Instruments myDAQ [4] (which also needs a computer as the virtual instrument), the ADALM 2000 [5], Analog Discovery 2 [6], and Red Pitaya [7]. All these relatively low-cost systems combine a function generator, oscilloscope, logic analyser and other instruments into a single package that costs less than $1000 (and as low as $300).

A typical system on chip (SoC) field-programmable gate array (FPGA) development board goes for less than $300. Pairing this with a $100 monitor or TV presents an affordable option for institutions. This, combined with the reconfigurability of FPGAs, served as the premise for this work. It is possible to use an FPGA board as lab equipment for one laboratory session, and a few minutes later, use it as a digital signal processor for processing multimedia or communications signals, and a few minutes after that, use it as a machine-learning classifier. We made use of a Terasic DE1-SoC Board running an Intel Cyclone V FPGA (cost: $220) and a 14-inch monitor (repurposed from a defunct computer, i.e., free) for this work.

## 2 EXISTING WORK

FPGAs have been ubiquitous in education and have been used in several use cases. The discussion below presents use cases that are related to this work.

### 2.1 Versatility

Several remote laboratories have been developed based on FPGAs. A remote laboratory is a physical laboratory that is accessed over a network or the internet to perform experiments. Remote labs are different from virtual labs in that they have actual physical equipment at the remote end, on which the experiments are run. In these FPGA remote laboratories, a laboratory server was connected to one or more FPGA boards. Students programmed these FPGAs remotely via computer or mobile device terminals. The results were also received via the same platform. One of the foremost online laboratories is the LabsLand system, developed initially at the University of Deusto [8]. In the LabsLand community, one of the major successes that has been recorded is the FPGA-based remote laboratory [9], [10]. In their model, an FPGA development board is used for the system under test. This model has also been used by other researchers [11]–[19].

FPGAs have also been used in power converter systems [20], [21], and for reconfigurable computing [22]–[25] because of their high speed and low power consumption. In reconfigurable computing, the FPGA is paired with a CPU. The CPU controls the

reprogramming of the FPGA, determining its functions at different times, according to what is needed.

## 2.2 Speed

Ref. [26] used an FPGA to increase the average speed of a measurement system in order to reduce noise. Ref. [27] used the FPGA for direct torque control due to the inherent speed of FPGAs. The execution time of their developed system was 2.93 μs, more than ten times faster than dSPACE 1104. Ref. [28] implemented an IIR filter on an FPGA for high-speed filtration of EEG signals. Ref. [29] implemented an advanced triggering scheme for oscilloscopes on an FPGA. This was set up external to the oscilloscope. Ref. [30] used the speed of FPGAs to create a system that simulates the transients of electromagnetic signals. Ref. [31] used FPGAs to simulate an orthogonal frequency division multiplexing (OFDM) system in order to measure channel parameters.

## 2.3 Lab equipment

Refs. [21], [22], [32]–[35] implemented digital oscilloscopes on FPGAs. Ref. [32] developed a low-cost oscilloscope on a Terasic (Altera) DE0 Board. The output was displayed on a VGA monitor (640x480). Ref. [22] developed a digital storage oscilloscope (DSO) capable of 400 kS/s with an analogue bandwidth of 100 MHz and 64 MB memory. Refs. [3] and [4] implemented 3D graphic visualizations for their FPGA-based oscilloscopes. Ref. [35] included a PS/2 mouse user input to the oscilloscope. Their oscilloscope had an analogue bandwidth of 80 MHz.

Refs. [36] and [37] created digital oscilloscopes on FPGAs capable of sampling signals with frequencies above those that typical oscilloscopes can handle. They did this by using different sample rates to sample the signal in question at different points in time during a period. The entire signal was then reconstructed from memory and plotted on a display.

Ref. [38] developed a spectrum analyser on a Virtex5 FPGA. They achieved a spectral resolution of 16 kHz with a sampling frequency of 33 MHz. They were able to achieve 50,000 FFT/s. Ref. [39] designed an FPGA-based signal generator capable of generating signals between 1 and 10 kHz and between 0.1 and 7.5 V. Ref. [40] created a waveform generator capable of 1 MHz and 10 MHz. Ref. [41] created a module for teaching telecommunications courses. The FPGA was programmed to do binary amplitude-shift keying, frequency-shift keying, and phase-shift keying. This was done on an Altera DE2 FPGA Board. Refs. [42] and [43] created quadrature phase-shift-keying (QPSK) modulators on FPGAs. Ref. [44] used FPGAs to implement pulse-width modulators and phase-angle-control systems while teaching them to students.

## 2.4 Summary

FPGAs are low-cost, low-power-consumption, versatile, reprogrammable devices. Educational and development boards have been created for some low-end FPGAs. These boards provide multiple I/O interfacing for the FPGAs, making them useful for several applications [45], as recent research has shown.

Our work focused on combining lab equipment so that the FPGA would serve different purposes, depending on the configuration chosen. We also focused on the limitations of the FPGA regarding its use as lab equipment, particularly in terms of

its signal measurement and characterization abilities, compared against standard lab equipment.

## 3 METHODOLOGY

A Terasic DE1-SoC board was used for this work. While the DE1-SoC board has an ARM microprocessor on board, the design implemented did not make use of it at all. Hence, the design used can be used on any FPGA board, with or without an embedded microprocessor on it. Programming of the board was done using VHDL. Figure 1 shows the block diagram of the FPGA lab instrument developed.

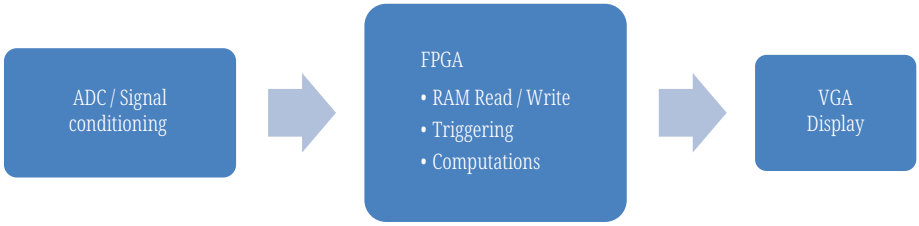



**Fig. 1.** Block diagram of the FPGA-based reconfigurable lab instrument

### 3.1 Data acquisition

The on-board analogue-to-digital converter (ADC) employed on the FPGA board is the LTC2308 chip. The LTC2308 ADC is an 8-channel, 12-bit ADC that produces 500 kilo-samples per second, though it is able to work with a 40-MHz clock. The on-board ADC is only able to reliably convert positive voltage signals between 0 V and 4 V (actually, about 4.2 V). While a signal-conditioning circuit could be built externally to clamp and scale larger voltage swings to this range, we opted against this, as the aim was to focus on the FPGA as a multi-instrument device in and of itself.

### 3.2 Data manipulation and storage

Displaying all the data being received directly from the ADC resulted in the data being displayed on the screen changing too rapidly to be useful. A trigger controller was implemented to mitigate this. With the trigger controller, the outputs from the ADC were stored only in the RAM when the ADC's output value matched the set trigger level. This led to a much less rapid change of the data in the RAM, hence leading to a steady display when plotted. The trigger function was also used for the computation of the signal's frequency. The period of the wave was measured by a counter, based on the time between intersections of the waveform and the trigger. The algorithms for triggering the oscilloscope and the frequency calculation were based on the work by Ref. [46]. These are presented in Figures 2 and 3.

The raw results from the ADC were sent to the RAM. In this work, two RAM buffers were created. The use of two separate buffers was to avoid the read-and-write collision that might occur when trying to read from and write to the same buffer simultaneously. The buffers were written to alternate, and data was read from the buffer not being written to. Thus, the two buffers allowed for glitch-free access to the ADC values. A RAM controller was implemented on the FPGA to determine the RAM buffer to read from and write to.

### 3.3 Instrument logic

A VHDL module was created to hold the required background graphics for display on the instrument display, and another was created for displaying text on the display. The background graphics and the text displays were defined in VHDL because they were both basic enough not to require the use of a memory-initialization file. It is worth noting that with an FPGA with fewer logic blocks, it might be better to read the text from memory, as this would minimize the logic blocks required to implement text on the screen. Drawing the grid on the screen, however, should always be defined in VHDL, as there is no gain in reading this from memory.

Two lab instruments were implemented on the FPGA: an oscilloscope and a digital multimeter. Switch SW0 was used to reset the board. Push button 3 was used to set the trigger value. There were nine preset trigger values: 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, and 4 V. Push button 3 cycled through these nine values when pressed.

Switch SW3 on the DE1-SoC board was used to select between the instruments. In the oscilloscope mode, the graduated chart onto which the data read from the RAM was plotted is displayed. Switches SW6 to SW9 were used to set the time base. In the multimeter mode, just text was displayed on the screen.

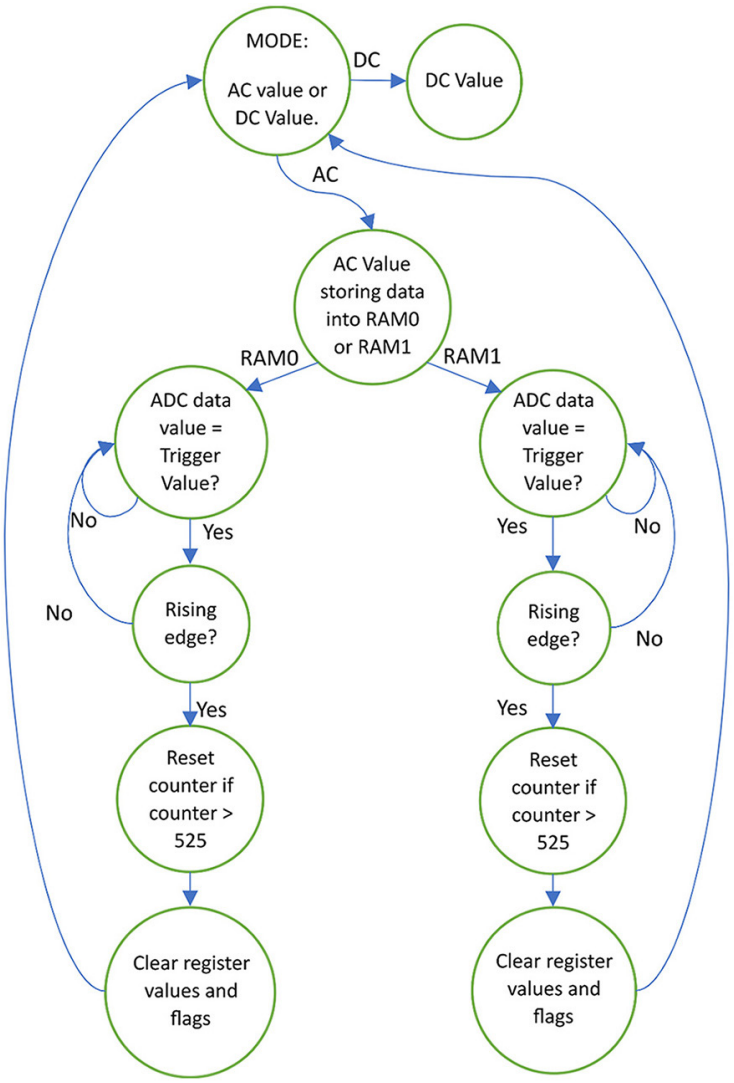



**Fig. 2.** The trigger function of the FPGA oscilloscope [46]

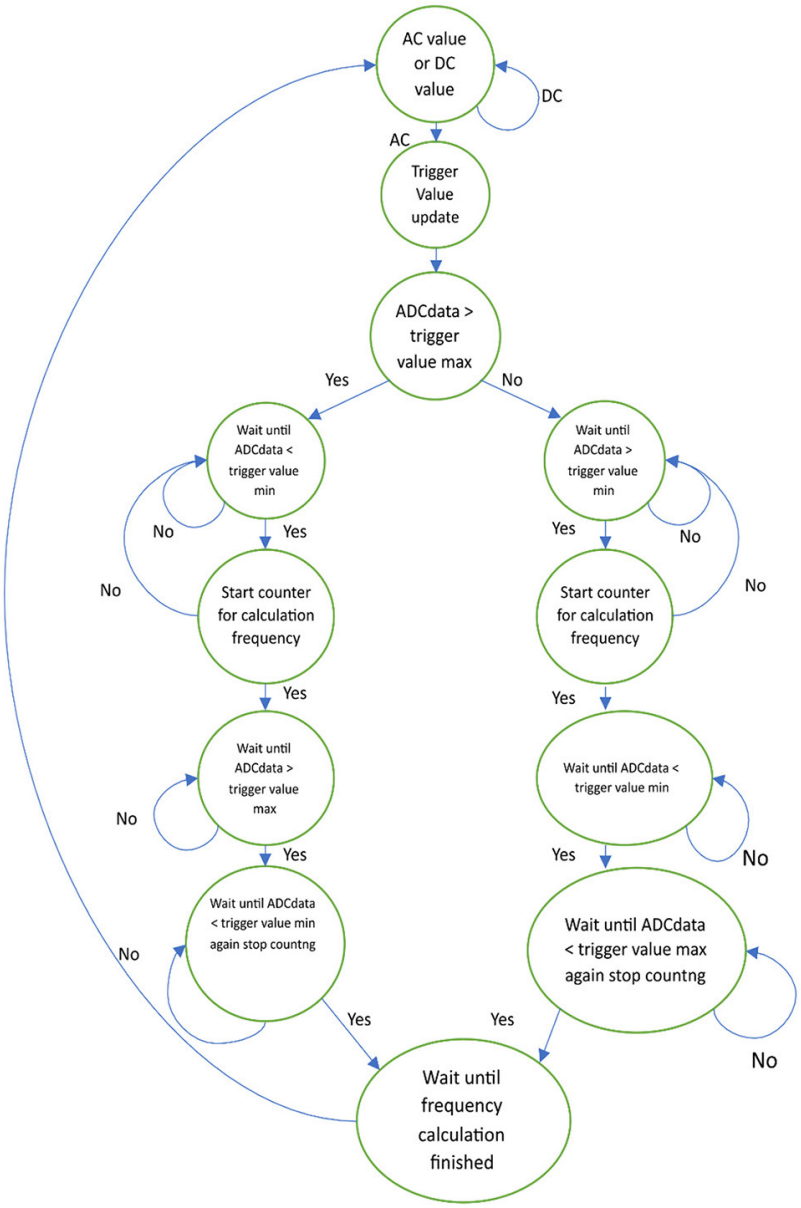



**Fig. 3.** Frequency calculation in the FPGA oscilloscopes [46]

The multimeter comes in handy when the user needs just the quantity (i.e., value) of the signal being measured, rather than the quality. The FPGA-based multimeter we developed is suited to measuring voltages. To measure other electrical quantities, such as resistance and current, external circuits would be built to convert the specific parameters to be measured into voltages. The developed multimeter measures the highest value and the lowest value of the time-varying signal at its input and computes the root mean square (RMS). These values are shown in the display.

## 3.4 Instrument display

A VGA (640 × 480 resolution) screen was used as the output of this work to display data on a screen. Specifically, a CRT computer monitor was used for this work. In keeping with the low-cost theme, no purchase was made since there was a computer

monitor not otherwise being used that was available for the work. This display size was kept as VGA to minimise the amount of memory needed to hold the data to be displayed. The waveform display area on the screen is 512 by 386 pixels. This was done for convenience, to match the display with the buffer size. The word length of the buffer was 512. Horizontal time scaling was achieved by changing the rate at which the ADC wrote values to the buffer.

## 3.5 Testing of the system

In testing our system, signals were supplied to our FPGA lab instrument and the output of the FPGA was displayed on a VGA monitor. Figure 4 shows the FPGA lab instrument coupled to a VGA display. The output of the FPGA was shown on the VGA. A standard function generator was used as the signal generator. A traditional digital oscilloscope was used as the "control" output to show the "standard measurement" for comparison. The testing was done in two phases. In the first phase, the FPGA instrument and the standard oscilloscope were connected in parallel, so that the input signal was supplied to both simultaneously. The goal here was to ensure that the measurements that were taken on the FPGA instrument could be compared directly against the standard oscilloscope. In the second phase, each instrument was used individually so that the input signal was supplied to one instrument at a time. In this way, it was possible to compare the input characteristics of the FPGA instrument with that of the standard oscilloscope. The goal here was to ensure that the results obtained in the first phase could be trusted, i.e., that connecting the FPGA instrument in parallel with the oscilloscope did not adversely affect the measurements of either instrument.

In both phases, in order the test the accuracy of the FPGA lab instrument, sine waves, square waves and triangle waves with peak-to-peak values between 0 and 4 V were supplied to the FPGA and the oscilloscope at frequencies between 10 Hz and 2 MHz. The results from the FPGA and from the traditional oscilloscope were recorded. Multiple readings were taken for each input and recorded.

The performance of the FPGA lab instrument was compared to the traditional oscilloscope and not to the source, the standard function generator, because the goal was to see the FPGA work in place of a traditional oscilloscope. By comparing the FPGA instrument to the oscilloscope, we could better determine the possibility of replacing the oscilloscope with the FPGA instrument.

(a)

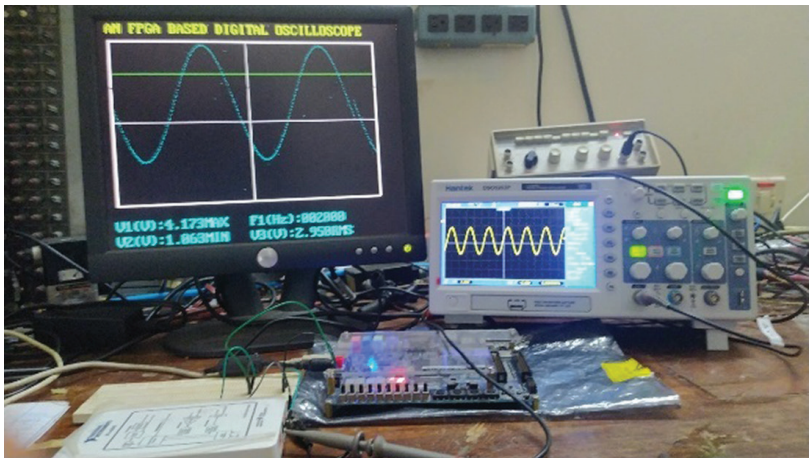
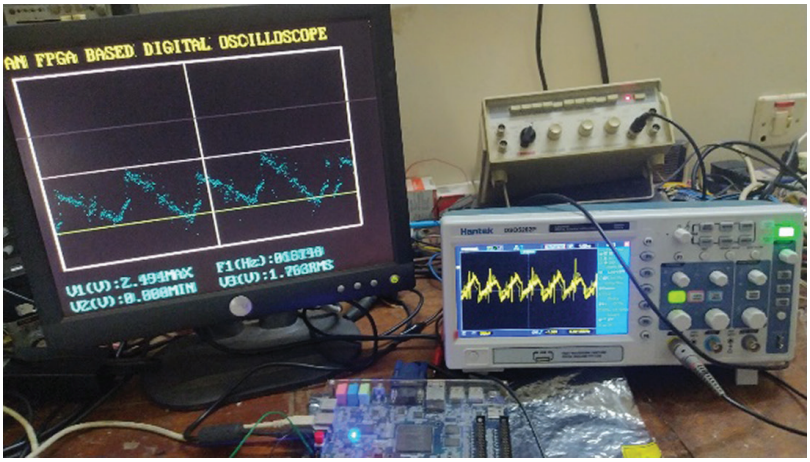



**Fig. 4.** *(Continued)*

(b)




(c)

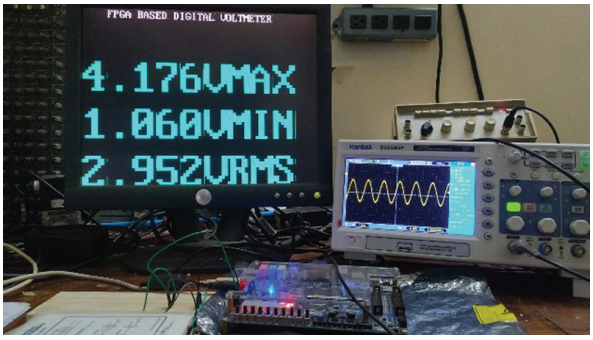



**Fig. 4.** The FPGA oscilloscope showing (a) a sinusoidal signal and (b) an arbitrary waveform, and (c) the FPGA digital voltmeter

No specific tests were done for the FPGA multimeter that we developed, because the FPGA multimeter was based on the code for the FPGA oscilloscope.

The Terasic DE1-SoC board that was used for this work makes use of an LTC2308 ADC. The specifications of this ADC, as provided by Terasic, state that the accepted input voltage range is 0 to 4 V. The tests performed here were therefore limited to this range to avoid damaging the board. However, it should be noted that signal processing can be used to condition input signals of any desired range to this range. For example, signals of the range of –10 to 10 V can be measured by first clamping up the signal and then scaling it down by a factor of 5 so that –10 V could be supplied as 0 V to the ADC and +10 V could be supplied as 4V. When displaying the results, the results could be displayed on the original scale of –10 to 10 V.

## 4 RESULTS AND DISCUSSION

The results from phase 1 of the testing are not presented here because they are not representative of the system. The measurements were always identical between the two instruments despite the input frequency. There was, however, marked disparity between the instruments' readings and the signal generator's settings at higher frequencies.

The mean recordings from phase 2 of the testing are presented in Tables 1 and 2. Table 1 shows the results for (relatively) low-frequency input signals. For the reporting of these results, we classify signals of 10 kHz and below as low-frequency signals and signals above this as high-frequency signals.

Table 1 clearly shows good correlation between the results of the FPGA instrument and the traditional oscilloscope. The mean error for the maximum voltage measurements was 0.0580 V, while the mean error for the minimum voltage measurement was 0.0133 V. The frequency measurement had a mean error of 3.65 Hz.

At high frequencies, however, as seen in Table 2, it seems that the input impedance of the FPGA system began to be an issue. The FPGA instrument's readings were all consistently below those of the traditional oscilloscope, with the error increasing with signal frequency. Figure 5 shows the measurement errors of the FPGA lab instrument. In Figure 6, the percentage error in the measurement of the maximum voltage is plotted against the frequency of the signal measured. The percentage error increased with frequency above about 15 kHz and exceeded 2% at about 100 kHz. Hence, we report that the FPGA lab instrument is sufficiently accurate for signals of frequencies below 100 kHz. This is consistent with previous works that reported an analogue bandwidth of 100 kHz.

As regards the resource utilisation of the Cyclone V FPGA for the implementation of these two lab instruments, 80% of the adaptive logic modules (ALMs) were used but just 13% of the digital signal processing blocks and less than 1% of the memory blocks. The details of the resource utilization are shown in Figure 7. The specifications of the MAX10 FPGA on a Terasic DE10-Lite board are: 49,760 programmable logic elements, 1,677,312 memory bits, 4 PLLs and 144 18´18 multipliers. This means that the system is easily deployable on the DE10-Lite board, which retails for $55 at the date of writing (for Academic use) [47]. Pairing this with a low-cost (or used) VGA display could mean having at least an oscilloscope and a digital multimeter for less than $100, though we are confident that at least a logic analyser can also be included with these two instruments on the DE10-Lite board.

**Table 1.** Low-frequency test results of FPGA oscilloscope vs. standard oscilloscope

| Signal Type | Standard Oscilloscope | | | FPGA Oscilloscope | | |
|---|---|---|---|---|---|---|
| | Freq (Hz) | $V_{max}$ (V) | $V_{min}$ (V) | Freq (Hz) | $V_{max}$ (V) | $V_{min}$ (V) |
| **Sine Wave** | 100 | 4.12 | 1.08 | 100 | 4.075 | 1.082 |
| | 500 | 4.12 | 1.08 | 500 | 4.075 | 1.082 |
| | 500 | 2.10 | 0.04 | 499 | 2.085 | 0.085 |
| | 955 | 4.16 | 0.80 | 954 | 4.052 | 0.741 |
| | 956 | 0.28 | 0.01 | 952 | 0.287 | 0.016 |
| | 956 | 1.08 | 0.13 | 956 | 1.087 | 0.136 |
| | 956 | 2.87 | 1.91 | 956 | 2.868 | 1.913 |
| | 9460 | 2.87 | 1.91 | 9440 | 2.868 | 1.913 |
| | 9461 | 4.18 | 0.80 | 9440 | 4.056 | 0.740 |
| | 15,000 | 2.10 | 0.06 | 14722 | 2.076 | 0.093 |
| | 94,790 | 4.14 | 0.82 | 100755 | 4.057 | 0.741 |
| **Triangular Wave** | 972 | 3.40 | 1.54 | 974 | 3.283 | 1.477 |
| | 974 | 3.40 | 1.54 | 974 | 3.290 | 1.470 |
| | 2008 | 4.06 | 0.84 | 2008 | 3.961 | 0.779 |
| | 2008 | 3.38 | 1.52 | 2008 | 3.291 | 1.470 |
| | 5000 | 2.10 | 0.06 | 5001 | 2.080 | 0.088 |
| | 5900 | 2.08 | 0.10 | 5884 | 2.050 | 0.117 |

*(Continued)*

**Table 1.** Low-frequency test results of FPGA oscilloscope vs. standard oscilloscope (*Continued*)

| Signal Type | Standard Oscilloscope | | | FPGA Oscilloscope | | |
|---|---|---|---|---|---|---|
| | Freq (Hz) | $V_{max}$ (V) | $V_{min}$ (V) | Freq (Hz) | $V_{max}$ (V) | $V_{min}$ (V) |
| **Square Wave** | 10 | 2.12 | 0.04 | 10 | 2.087 | 0.082 |
| | 100 | 2.16 | 0.04 | 100 | 2.087 | 0.083 |
| | 972 | 3.50 | 1.42 | 970 | 3.388 | 1.358 |
| | 5000 | 2.12 | 0.06 | 5001 | 2.083 | 0.082 |
| | 9634 | 3.50 | 1.42 | 9622 | 3.388 | 1.360 |

**Table 2.** High-frequency test results of FPGA oscilloscope vs. standard oscilloscope

| Signal Type | Freq (Hz) | Standard Oscilloscope | | FPGA Oscilloscope | |
|---|---|---|---|---|---|
| | | $V_{max}$ (V) | $V_{min}$ (V) | $V_{max}$ (V) | $V_{min}$ (V) |
| **Sine Wave** | 15,000 | 2.1 | 0.06 | 2.076 | 0.093 |
| | 94,790 | 4.14 | 0.82 | 4.057 | 0.741 |
| | 228,100 | 4.16 | 0.84 | 4.052 | 0.745 |
| | 985,200 | 4.02 | 0.96 | 3.88 | 0.901 |
| | 2,011,000 | 3.72 | 1.28 | 3.477 | 1.312 |
| **Triangular Wave** | 14,980 | 2.02 | 0.14 | 2.003 | 0.168 |
| | 96,620 | 3.38 | 1.54 | 3.296 | 1.466 |
| **Square Wave** | 15,000 | 2.12 | 0.06 | 2.083 | 0.083 |
| | 96,550 | 3.5 | 1.42 | 3.391 | 1.356 |

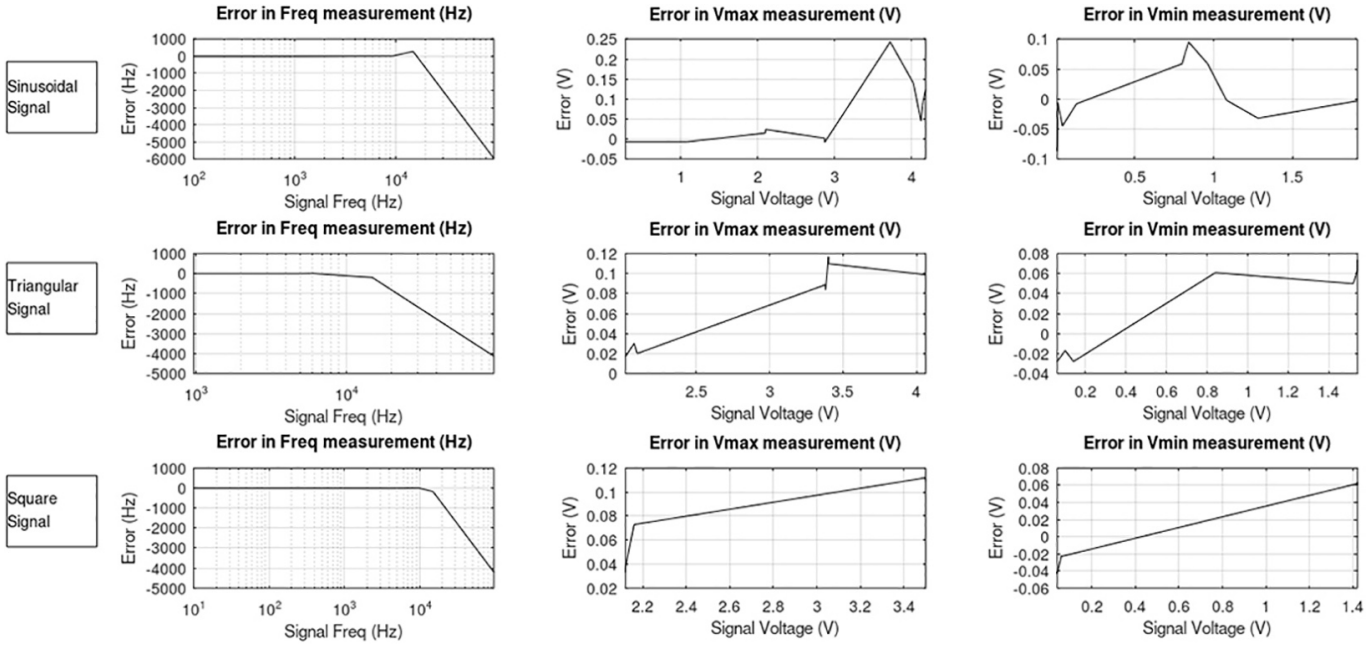



**Fig. 5.** Measurement errors for low-frequency measurements

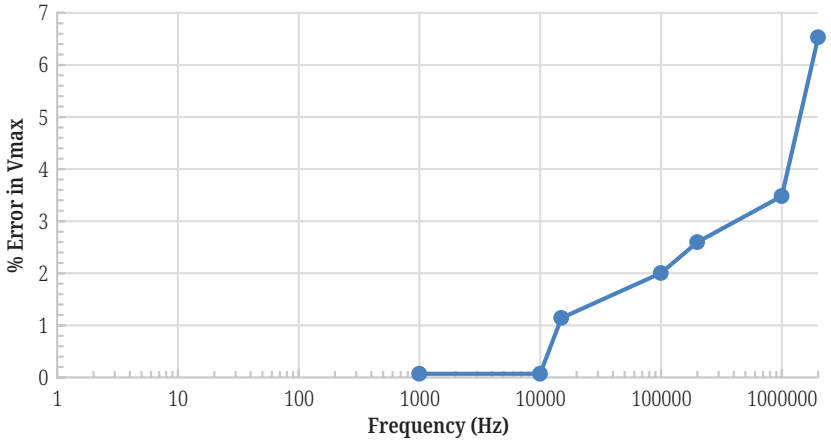



**Fig. 6.** Percent error in FPGA instrument in maximum voltages measured at various frequencies

| | |
|---|---|
| Quartus Prime Version | 20.1.0 Build 711 06/05/2020 SJ Lite Edition |
| Revision Name | digitaloscilloscope |
| Top-level Entity Name | digitaloscilloscope |
| Family | Cyclone V |
| Device | 5CSEMA5F31C6 |
| Timing Models | Final |
| Logic utilization (in ALMs) | 25,765 / 32,070 ( 80 % ) |
| Total registers | 13089 |
| Total pins | 60 / 457 ( 13 % ) |
| Total virtual pins | 0 |
| Total block memory bits | 0 / 4,065,280 ( 0 % ) |
| Total DSP Blocks | 11 / 87 ( 13 % ) |
| Total HSSI RX PCSs | 0 |
| Total HSSI PMA RX Deserializers | 0 |

**Fig. 7.** Resource utilization of the Cyclone V for the lab instruments developed

## 5 CONCLUSION

This project is a demonstration of the use of an FPGA board as a replacement to laboratory equipment. Our goal was to determine the accuracy and ability of the FPGA-based instruments to confirm that the concept was sound. The next step would be to reduce the cost of the laboratory equipment replacement even further by making use of a smaller, less expensive board e.g., the Intel DE10-Lite. Less than 42% of the configurable logic blocks on the Cyclone V FPGA on the DE1-SoC board were used for the implementation of the oscilloscope and the digital multimeter. Implementing these on the DE10-Lite board would reduce the cost of the system by about $120. A further step would be to increase the number of laboratory

instruments available on the DE1-SoC; for example, include a spectrum analyser and a logic analyser. However, we have no plan to replace the function generators in the laboratory with FPGA-based systems. This is because that while the FPGA can easily be programmed to generate various functions and arbitrary waveforms, it is limited in the amount of power that it can output. Hence, it would need to be paired with a power amplification setup (a driver circuit) to be able to drive most loads used in laboratory sessions. The code developed for this work is openly available on GitHub at https://github.com/wale2oba/FPGA-Lab-Instrument.

## 6 ACKNOWLEDGMENT

We would like to acknowledge the Intel Corporation, USA, for their donation of the Terasic DE1-SoC board to our department for teaching.

## 7 REFERENCES

[1] L. D. Feisel, G. D. Peterson, O. Arnas, L. Carter, A. Rosa, and W. Worek, "Learning objectives for engineering education laboratories", in *32nd Annual Frontiers in Education*, Nov. 2002, pp. F1D-. https://doi.org/10.1109/FIE.2002.1158127

[2] L. D. Feisel and A. J. Rosa, "The role of the laboratory in undergraduate engineering education", *Journal of Engineering Education*, vol. 94, pp. 121–130, 2005. https://doi.org/10.1002/j.2168-9830.2005.tb00833.x

[3] Y. Yan, R. Adams, P. Yanik, H. Jack, A. Ritenour, and H. Karayaka, "BYOE: Individual Lab Kit Options for Analog and Digital Circuits Suitable for In-class or At-home Experiments", in *2021 ASEE Virtual Annual Conference Content Access Proceedings*, Virtual Conference: ASEE Conferences, Jul. 2021, p. 36778. https://doi.org/10.18260/1-2--36778

[4] "myDAQ Student Data Acquisition Device – NI". https://www.ni.com/en-za/shop/hardware/products/mydaq-student-data-acquisition-device.html (accessed Apr. 18, 2023).

[5] "ADALM2000 Evaluation Board | Analog Devices". https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/adalm2000.html (accessed Apr. 18, 2023).

[6] "Analog Discovery 2: 100MS/s USB Oscilloscope, Logic Analyzer and Variable Power Supply", *Digilent*. https://digilent.com/shop/analog-discovery-2-100ms-s-usb-oscilloscope-logic-analyzer-and-variable-power-supply/ (accessed Apr. 18, 2023).

[7] "Red Pitaya – Swiss Army Knife For Engineers", May 03, 2021. https://redpitaya.com/ (accessed Apr. 18, 2023).

[8] P. Orduña, L. Rodriguez-Gil, J. Garcia-Zubia, I. Angulo, U. Hernandez, and E. Azcuenaga, 'LabsLand: A sharing economy platform to promote educational remote laboratories maintainability, sustainability and adoption", in *2016 IEEE Frontiers in Education Conference (FIE)*, Oct. 2016, pp. 1–6. https://doi.org/10.1109/FIE.2016.7757579

[9] C. A. Mayoz, A. L. da Silva Beraldo, A. Villar-Martinez, L. Rodriguez-Gil, W. F. M. de Souza Seron, and P. Orduña, "FPGA remote laboratory: experience of a shared laboratory between UPNA and UNIFESP", in *2020 XIV Technologies Applied to Electronics Teaching Conference (TAEE)*, Jul. 2020, pp. 1–8. https://doi.org/10.1109/TAEE46915.2020.9163773

[10] J. García-Zubía, I. Angulo, L. Rodriguez-Gil, P. Orduña, O. Dziabenko, and M. Güenaga, "Boole-WebLab-FPGA: Creating an integrated digital electronics learning workflow through a hybrid laboratory and an educational electronics design tool", *International Journal of Online and Biomedical Engineering (iJOE)*, vol. 9, pp. 19–22, 2013. https://doi.org/10.3991/ijoe.v9iS8.3362

[11] K. P. Ayodele, O. B. Akinwale, L. O. Kehinde, O. Osasona, E. O. B. Ajayi, and O. O. Akinwunmi, "Advanced Digital Laboratory: An Fpga Based Remote Laboratory for Teaching Digital Electronics", presented at the 2009 Annual Conference & Exposition, Jun. 2009, p. 14.163.1–14.163.13. Accessed: Oct. 29, 2018. [Online]. Available: https://peer.asee.org/advanced-digital-laboratory-an-fpga-based-remote-laboratory-for-teaching-digital-electronics

[12] N. Fujii and N. Koike, "IoT Remote Group Experiments in the Cyber Laboratory: A FPGA-based Remote Laboratory in the Hybrid Cloud", in *2017 International Conference on Cyberworlds (CW)*, Sep. 2017, pp. 162–165. https://doi.org/10.1109/CW.2017.29

[13] R. Hashemian and J. Riddley, "FPGA e-Lab, a Technique to Remote Access a Laboratory to Design and Test", in *2007 IEEE International Conference on Microelectronic Systems Education (MSE"07)*, Jun. 2007, pp. 139–140. https://doi.org/10.1109/MSE.2007.43

[14] Y. Toyoda, N. Koike, and Y. Li, "An FPGA-based remote laboratory: Implementing semi-automatic experiments in the hybrid cloud", in *2016 13th International Conference on Remote Engineering and Virtual Instrumentation (REV)*, Feb. 2016, pp. 24–29. https://doi.org/10.1109/REV.2016.7444435

[15] W. M. El-Medany, "FPGA remote laboratory for hardware e-learning courses", in *2008 IEEE Region 8 International Conference on Computational Technologies in Electrical and Electronics Engineering*, Jul. 2008, pp. 106–109. https://doi.org/10.1109/SIBIRCON.2008.4602596

[16] R. J. Costa, D. E. Pinho, and G. R. Alves, "Using embedded instruments to design web-labs: An FPGA-embedded oscilloscope based on the IEEE1451.0 Std.", in *2015 3rd Experiment International Conference (exp.at'15)*, Jun. 2015, pp. 41–46. https://doi.org/10.1109/EXPAT.2015.7463211

[17] R. J. Costa, G. R. Alves, and M. Z. Rela, "Embedding instruments & modules into an IEEE1451-FPGA-based Weblab infrastructure", *International Journal of Online and Biomedical Engineering (iJOE)*, vol. 8, no. 3, 2012. https://doi.org/10.3991/ijoe.v8i3.2064

[18] A. Kalantzopoulos, E. Galetakis, C. Katsenos, and E. Zigouris, "An interactive remote laboratory on basic computer architecture using Altera DE2 board", *International Journal of Online and Biomedical Engineering (iJOE)*, vol. 9, no. 5, 2013. https://doi.org/10.3991/ijoe.v9i5.2675

[19] S. Gadzhanov, A. Nafalski, and Z. Nedic, "Remote laboratory for advanced motion control experiments", *International Journal of Online and Biomedical Engineering (iJOE)*, vol. 10, no. 5, 2014. https://doi.org/10.3991/ijoe.v10i5.3835

[20] A. Agarwal, M. Karmakar, and V. Agarwal, "Design of FPGA based controller for trapezoidal modulated cycloinverter", in *2010 Fifth International Conference on Information and Automation for Sustainability*, Dec. 2010, pp. 479–483. https://doi.org/10.1109/ICIAFS.2010.5715709

[21] F. Pereira, L. Gomes, and L. Redondo, "FPGA controller for power converters with integrated oscilloscope and graphical user interface", in *2011 International Conference on Power Engineering, Energy and Electrical Drives*, May 2011, pp. 1–6. https://doi.org/10.1109/PowerEng.2011.6036436

[22] He Zhiqiang, Feng Guonan, and Zhang Jingzhi, "Design and implement of the digital storage oscilloscope card based on VHDL", in *IEEE 2011 10th International Conference on Electronic Measurement Instruments*, Aug. 2011, pp. 346–349. https://doi.org/10.1109/ICEMI.2011.6037747

[23] D. Ji-Jie, S. Fa, H. Li-Li, and W. Wei, "Research on dynamic reconfigurable based on FPGA", *Ferroelectrics*, vol. 548, no. 1, pp. 177–184, 2019. https://doi.org/10.1080/00150193.2019.1592524

[24] I. A. Kalyaev, I. I. Levin, A. I. Dordopulo, and L. M. Slasten, "FPGA-based reconfigurable computer systems", in *2013 Science and Information Conference*, Oct. 2013, pp. 148–155.

[25] Y. Verbelen, P. Taelman, A. Braeken, and A. Touhafi, "Reconfigurable and modular mobile robotics platform for remote experiments", *International Journal of Online and Biomedical Engineering (iJOE)*, vol. 9, no. 3, 2013. https://doi.org/10.3991/ijoe.v9i3.2554

[26] X. Bo, Y. Yunpeng, C. Kai, Y. Yanjun, Z. Shuo, and W. Yifan, "An efficient waveform averaging method based on FPGA in oscilloscope", in *2019 14th IEEE International Conference on Electronic Measurement Instruments (ICEMI)*, Nov. 2019, pp. 124–131. https://doi.org/10.1109/ICEMI46757.2019.9101595

[27] S. Krim, S. Gdaim, A. Mtibaa, and M. F. Mimouni, "Control with high performances based DTC strategy: FPGA implementation and experimental validation", *EPE Journal*, vol. 29, no. 2, pp. 82–98, 2019. https://doi.org/10.1080/09398368.2018.1548802

[28] A. Mahabub, "Design and implementation of cost-effective IIR filter for EEG signal on FPGA", *Australian Journal of Electrical and Electronics Engineering*, vol. 17, no. 2, pp. 1–9, 2020. https://doi.org/10.1080/1448837X.2020.1771662

[29] S. A. Khan, A. K. Agarwala, and D. T. Shahani, "Implementation of Advance Oscilloscope Triggering Scheme on FPGA", in *2005 IEEE Instrumentationand Measurement Technology Conference Proceedings*, May 2005, pp. 407–411. https://doi.org/10.1109/IMTC.2005.1604147

[30] X. Zhou, G. He, and X. Zhou, "FPGA Design and Implementation for Real-Time Electromagnetic Transient Simulation System", in *2015 IEEE 17th International Conference on High Performance Computing and Communications, 2015 IEEE 7th International Symposium on Cyberspace Safety and Security, and 2015 IEEE 12th International Conference on Embedded Software and Systems*, Aug. 2015, pp. 848–851. https://doi.org/10.1109/HPCC-CSS-ICESS.2015.309

[31] A. Pramanik and P. Banerjee, "Measurement of real channel parameters of FPGA based OFDM system", in *International Conference on Electronics, Communication and Instrumentation (ICECI)*, Jan. 2014, pp. 1–4. https://doi.org/10.1109/ICECI.2014.6767368

[32] B. Başa and M. İskefiyeli, "Realization of Digital Oscilloscope with FPGA for Education", *Procedia – Social and Behavioral Sciences*, vol. 174, pp. 814–820, 2015. https://doi.org/10.1016/j.sbspro.2015.01.666

[33] M. A. Hossin, S. A. Rahman, P. Ye, and Y. Xiaohua, "User Selectable Brightness Control and Adjustment of 3D Digital Oscilloscope", in *2018 International Conference on Audio, Language and Image Processing (ICALIP)*, Jul. 2018, pp. 210–215. https://doi.org/10.1109/ICALIP.2018.8455732

[34] N. Hu, X. Zhou, X. Li, and C. Wang, "3D Waveform Oscilloscope Implemented on Coupled FPGA-GPU Embedded System", in *2018 5th International Conference on Information Science and Control Engineering (ICISCE)*, Zhengzhou: IEEE, Jul. 2018, pp. 1–5. https://doi.org/10.1109/ICISCE.2018.00010

[35] S. K. Pal, A. Kumar, and K. Kumawat, "Design and VLSI Implementation of a Digital Oscilloscope", in *2012 Fourth International Conference on Computational Intelligence and Communication Networks*, Nov. 2012, pp. 473–476. https://doi.org/10.1109/CICN.2012.88

[36] A. Afaneh, H. Yin, and A. N. Kalashnikov, "Implementation of accurate frame interleaved sampling in a low cost FPGA-based data acquisition system", in *Proceedings of the 6th IEEE International Conference on Intelligent Data Acquisition and Advanced Computing Systems*, Sep. 2011, pp. 20–25. https://doi.org/10.1109/IDAACS.2011.6072703

[37] Y. Wanyu, Z. Yijiu, Y. Zhonghao, and L. Dan, "Design of random equivalent sampling control module based on FPGA", in *2019 14th IEEE International Conference on Electronic Measurement Instruments (ICEMI)*, Nov. 2019, pp. 1027–1032. https://doi.org/10.1109/ICEMI46757.2019.9101501

[38] R. Borade, A. Dimber, D. Gharpure, and S. Ananthakrishnan, "Design and development of FPGA-based spectrum analyzer", *IETE Journal of Education*, vol. 59, no. 1, pp. 5–17, 2018. https://doi.org/10.1080/09747338.2018.1450648

[39] S. Jie, Y. Hang, G. Chengbin, L. Teng, and H. You, "Design and implementation of signal generator and real-time analysis system", in *2013 25th Chinese Control and Decision Conference (CCDC)*, May 2013, pp. 4517–4520. https://doi.org/10.1109/CCDC.2013.6561749

[40] P. Sun and M. Jin, "Synthetic Waveform Generator for Filter Application Based on FPGA", in *2015 Ninth International Conference on Frontier of Computer Science and Technology*, Aug. 2015, pp. 161–165. https://doi.org/10.1109/FCST.2015.62

[41] C. Erdoğan, I. Myderrizi, and S. Minaei, "FPGA implementation of BASK-BFSK-BPSK digital modulators", *IEEE Antennas and Propagation Magazine*, vol. 54, no. 2, pp. 262–269, Apr. 2012. https://doi.org/10.1109/MAP.2012.6230771

[42] R. Deepika, S. KS, and M. J, "Design and Implementation of a novel QPSK demodulator for FPGA based system design", in *2019 IEEE International WIE Conference on Electrical and Computer Engineering (WIECON-ECE)*, Nov. 2019, pp. 1–4. https://doi.org/10.1109/WIECON-ECE48653.2019.9019948

[43] S. O. Popescu, A. S. Gontean, and D. Ianchis, "QPSK Modulator on FPGA", in *2011 IEEE 9th International Symposium on Intelligent Systems and Informatics*, Sep. 2011, pp. 359–364. https://doi.org/10.1109/SISY.2011.6034353

[44] D. H. Badarov and V. D. Manoev, "Teaching methodology for digital pulse width modulation and phase angle control", in *2017 XXVI International Scientific Conference Electronics (ET)*, Sep. 2017, pp. 1–4. https://doi.org/10.1109/ET.2017.8124335

[45] C.-G. Haba, "Using FPGA development boards for multi-course laboratory support", in *2014 IEEE Global Engineering Education Conference (EDUCON)*, Apr. 2014, pp. 794–797. https://doi.org/10.1109/EDUCON.2014.6826185

[46] H. Jin, "Digital Scope Implemented on Altera DE1-SoC", Cornell University, School of Electrical and Computer Engineering, MEng. Project Report, May 2016. [Online]. Available: https://people.ece.cornell.edu/land/courses/eceprojectsland/STUDENTPROJ/2015to2016/hj424/hj424_report_201605191237.pdf

[47] Terasic Inc., "DE10-Lite Board", *Terasic*. https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=218&No=1021&PartNo=2 (accessed Sep. 10, 2020).

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