Simulation Analysis of Improved Construction and Control Strategy for Programmable AC Power Source

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***Abstract*—Novel circuit topology and advanced control technique of inverter are research focus for programmable AC power source. An improved dual buck half bridge inverter topology is introduced and the central symmetrical pulse width modulation mode is proposed to double the output current ripple frequency. High output precision can be achieved by optimizing the output waveforms of inverter. Then, a hybrid digital control scheme combining PID control with repetitive control as well as inductance compensation deadbeat control is presented for the closed loop voltage regulation of the mentioned inverter. Besides, an inductance saturation characteristic mathematic model is established for accurate simulation. Simulation results show that the theoretical analysis of the special switching sequence and hybrid control scheme is true.**

***Index Terms*—Programmable AC power source, PID control, Deadbeat control, Simulation**

I. INTRODUCTION

The design specifications of Programmable AC power source (PACS) are more rigid than the project specifications of other AC power conditioning systems such as uninterruptible power supply (UPS) and voltage automatic regulator. For example, a typical specification of total harmonic distortion (THD) of an UPS system for 60Hz line voltage regulation is below 5.0%. Under the same load condition, a PACS system is usually required to provide the output waveforms with lower THD 3.0% maximum [1].

In general, a PACS system consists of an isolated AC/DC converter and bridge type inverter which is the kernel component for PACS [2]. The conventional bridge type inverter topology has some inevitable problems that dead-zone state need to be added to switching sequence to avoid the probability of shoot-through currents. The dual buck half bridge inverter topology consisting of two buck converters solves the shoot-through problem and allows the zero dead-zone time operation [3]. This topology can not only ensure the reliability of inverter but also allow the available optimum design of switches and freewheel diodes respectively since the body diodes of switches never conduct current anytime [4-6]. Therefore, this paper proposes a dual buck half bridge topology with three inductors and the central symmetrical switching sequence of the two power switches so as to realize high output precision of inverter by the optimization of output current waveform for PACS system.

Referring to control strategy of inverter, many researches have focused on the closed loop regulation of pulse width modulated (PWM) inverter based on various digital control techniques to achieve fast dynamic response and low harmonic distortion. A fully digital multiple loop control scheme for the regulation of PWM inverter has been applied to AC power sources. And that the digital controller has been designed with deadbeat control theory to achieve fast dynamic response [7, 8]. Except for deadbeat control, the control approaches involve PID control [9, 10], repetitive control[11,12], instantaneous feedback control, sliding mode control and so on [13, 14].

Deadbeat control is a digital control method with the ability of precisely tracking reference in real time. However, the approach has high sensitivity to model uncertainties and parameter mismatches which factors reduce the performance of control system [15]. In this study, the inner current loop of PWM inverter should have the ultra-fast tracking ability, so deadbeat control is a better choice. This paper presents an inductance compensation scheme for the optimization of deadbeat controller. Thus, an inductance mathematic model and compensation control methods are built for simulation.

Considering the high applicability and rigid design specification of PACS, this paper presents a hybrid digital control scheme for the voltage regulation of the dual buck inverter. Except for the mentioned control techniques, the proposed digital control scheme includes the output voltage decoupling mechanism and load disturbance compensation scheme. Finally, the simulation results verify the validity of the topology analysis and control scheme.

II. CENTRAL SYMMETRICAL PWM

Fig.1 shows the proposed topology of dual buck inverter for programmable AC sources. V_{bus+} and V_{bus-} are the positive and negative BUS voltage respectively. L_1 and L_3 are filter inductors with the same inductance value, while L_2 is additive filter inductor which working frequency is doubled the switching frequency. i_1, i_2 and $i_1 - i_2$ are the current through the filter inductors L_1, L_2 and L_3 respectively. r_1 and r_2 are the equivalent series resistor of L_1 (L_3) and L_2 respectively. Z is the output impedance of the concerned power source. C is the output filter capacitance and V_0 is the output voltage. S1

and d_1 are on the same bridge arm, while S2 and d_2 are on the other one.

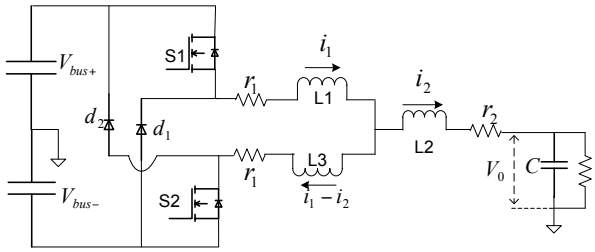

Fig.1 Improved dual buck half bridge inverter

The topology consists of two simple buck converters and has some substantial properties. For instance, the shoot-through is limited by the in-series inductors so zero dead-zone time operation is allowed. Even the two switches can work at the same time.

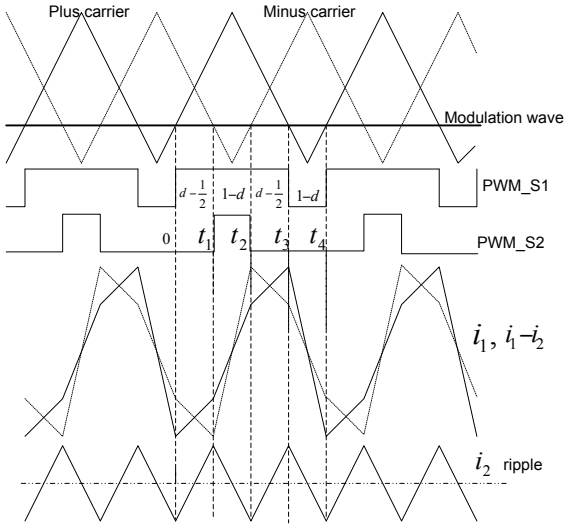

Fig.2 Two switching duty sequence and inductor current waveforms

Fig.2 shows central symmetrical switching sequence of the two switches and current ripple waveforms of the three inductors. The assumption is made that the two switches operate in relatively high switching frequency in comparison with the inverter output frequency and the three filter inductors all work in continuous current mode. Generally, the modulation technique always ensures that the top and bottom switches of the same bridge leg are gated alternately for traditional bridge type inverter. However, the suggested modulation mode will ensure that the two switches of this dual buck circuit are gated with central symmetrical switching sequence mode. Besides, when the duty of one switch is d, the duty of the other will be $1-d$. The sum total switching duty is maintained at unity. When the special duty distribution sequence is used, the result is that the current ripple frequency of L_2 is doubled and the output current ripple amplitude is greatly reduced. Summarily, the high output precision is realized by optimizing the output current waveform. The high precision of inverter is always required for programmable AC power source.

Theoretically, the switching frequency is virtually doubled due to a doubling of output current ripple frequency. When used as AC power source, the inverter often requires fairly high switching frequency to provide ample bandwidth for a high level of control precision. Therefore, the doubled virtual switching frequency results in higher-quality output voltage waveforms.

To further go into the research, the mathematical model of the PWM inverter will be derived. According to the improved dual buck half bridge circuit shown in Fig.1 and duty sequence of the two switches shown in Fig.2, the dynamic equations of the PWM inverter can be deduced. In one whole working cycle, four different modes of switching state are expressed by the equations (1), (2) and (3).

In $0 \sim t_1(d-\frac{1}{2})$ and $t_2 \sim t_3(d-\frac{1}{2})$, S1 is on and S2 is off,

$$\begin{cases} L_1\dfrac{di_1}{dt}+r_1i_1+L_2\dfrac{di_2}{dt}+r_2i_2=V_{bus+}-V_0 \\ -L_1\dfrac{d(i_1-i_2)}{dt}-r_1(i_1-i_2)=-L_2\dfrac{di_2}{dt}-r_2i_2-V_0+V_{bus+} \end{cases} \quad (1)$$

In $t_1 \sim t_2(1-d)$, S1 and S2 are both on,

$$\begin{cases} L_1\dfrac{di_1}{dt}+r_1i_1+L_2\dfrac{di_2}{dt}+r_2i_2=V_{bus+}-V_0 \\ L_1\dfrac{d(i_1-i_2)}{dt}+r_1(i_1-i_2)=L_2\dfrac{di_2}{dt}+r_2i_2+V_0+V_{bus-} \end{cases} \quad (2)$$

In $t_3 \sim t_4(1-d)$, S1 and S2 are both off,

$$\begin{cases} -L_1\dfrac{di_1}{dt}-r_1i_1-L_2\dfrac{di_2}{dt}-r_2i_2=V_{bus-}+V_0 \\ -L_1\dfrac{d(i_1-i_2)}{dt}-r_1(i_1-i_2)=-L_2\dfrac{di_2}{dt}-r_2i_2-V_0+V_{bus+} \end{cases} \quad (3)$$

Order $V_{bus+}=V_{bus-}=V_{bus}$, and $K_{pwm}=V_{bus}/V_t$. After adding the load current equation, the steady-state relation between output voltage and modulation wave is derived as

$$\frac{V_0(s)}{V_m(s)}=\frac{K_{pwm}}{(\frac{L_1}{2}+L_2)CS^2+[\frac{L_1+2L_2}{2Z}+C(\frac{r_1+2r_2}{2})]S+1+\frac{r_1+2r_2}{2Z}} \quad (4)$$

III. HYBRID CONTROL SCHEME

Fig.3 depicts a hybrid digital control theme for the proposed dual buck half bridge inverter. The proposed control scheme incorporates an inner current loop with an outer voltage loop to regulate the output voltage of the inverter. To improve the robustness of the mentioned inverter, the digital control adopts an output voltage decoupling mechanism as well as load disturbance compensation scheme. Since many types of loads may be connected to the AC power source, the load current will act as a disturbance to the outer voltage loop. The disturbance of load current can be compensated as a part of inductor current command in advance so as to suppress

the effect of load variation on the voltage distortion. Also, the interference of output voltage in the inner current loop can be suppressed by this means of output voltage feed-forward so as to improve the performance of current loop.

The deadbeat controller with an inductance compensation scheme is applied to the current loop. A two-layer control scheme including digital PID controller and repetitive controller is used in the voltage loop.

A. Current-Loop Controller Design

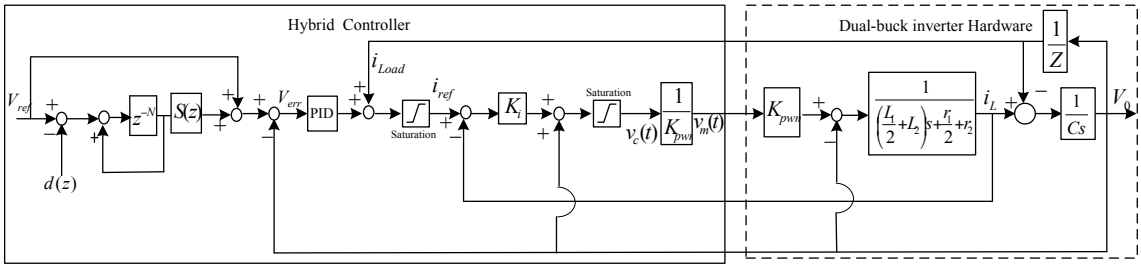

Fig.3 Block diagram of proposed hybrid control for AC voltage regulation

Since the output voltage feed-forward decoupling mechanism is applied, the model of the inner current loop can be simplified as shown in Fig.4, where L stands for $0.5L_1 + L_2$, r stands for $0.5r_1 + r_2$.

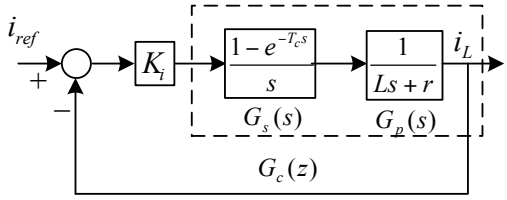

Fig.4 Simplified block diagram of the inner current loop

The discrete-time transfer function of the system $G_c(z)$ can be written as

$$G_c(z) = Z\left[(\frac{1-e^{-T_c s}}{s})*(\frac{1}{Ls+r})\right] = \frac{1}{r}*\frac{1-e^{-aT_c}}{z-e^{-aT_c}} \tag{5}$$

Where T_c is the sampling period of the digital current loop and $a = r/L$.

The characteristic equation of the closed current loop is obtained as

$$z - \left[e^{-aT_c} - K_i(\frac{1-e^{-aT_c}}{r})\right] = 0 \tag{6}$$

In order to achieve the deadbeat effect of closed loop system, the root of the characteristic equation is set at zero. Thus, the deadbeat gain K_i is designed as

$$K_i = \frac{re^{-aT_c}}{1-e^{-aT_c}} \tag{7}$$

Deadbeat control needs precise control model. Therefore, an inductance compensation scheme is presented to suppress the influence of inductance variation on control performance. Fig.5 shows the inductance saturation characteristic of the inductor made of amorphous alloy cores. The inductance value of L bears nonlinear variation with inductor current and it also has saturation characteristic under a certain current condition, as a result, the coefficient a is a variable resulting from current variation.

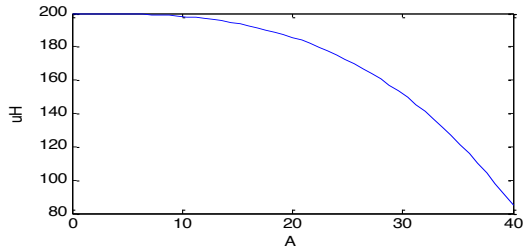

Fig.5 Nonlinear relation between the inductor current and inductance

According to the correlation between the inductor current and inductance, a lookup table can be built to give the real inductance to the deadbeat controller. Thus, the inductance compensation coefficient K_{com} is designed as

$$K_{com} = \frac{Table[i]}{L_0} \tag{8}$$

Where L_0 is the original inductance of the inductor, $Table[i]$ is the real inductance when the current flowing across the inductor reaches the value i. Then the deadbeat control coefficient a is modified as

$$a = \frac{r}{Table[i]} \tag{9}$$

B. Voltage-Loop Controller Design

Since the designed inner loop can precisely track the current command in real time, the loop can be regarded as a constant gain when designing the outer loop controller. After neglecting the dynamic of inner loop and compensating the load disturbance, the model of outer voltage loop can be simplified as shown in Fig.6. The two-layer control scheme for the voltage loop is based on digital PID control and repetitive control.

The PID algorithm is used to adjust the tracking errors of the output voltage in real time and reduce fluctuation and distortion of the waveform when the inverter system is interfered.

Discrete repetitive controller is used to eliminate the periodic tracking errors of the inverter system and reduces distortion of the output waveform. The function of repetitive controller is to improve the steady characteristics, while the function of PID controller mainly improves the transient response.

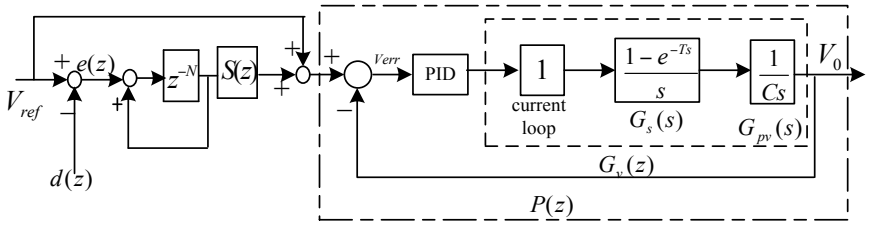

Fig.6 Simplified block diagram of the outer voltage loop

The PID controller is effective when the inverter system is interfered. However, the voltage errors are very small when the system is running in a steady state. At this time, the PID controller gives minor contribution to the running system in comparison with the repetitive controller. As a result of accumulating historical errors for periodic disturbances, the repetitive controller helps to the improvement of output waveform quality. So, when the running system experiences substantial disturbances, repetitive controller takes no effect due to a reference periodic delay. When this dynamic is ended, the repetitive controller become effective and tracking errors decrease rapidly. With the decrease of tracking errors, the effect of PID controller is gradually weakened until the system reaches a new steady state. Essentially, the two controllers are coupled and influenced each other. For the repetitive controller, the appropriate tuning of the convergent rate can minimize the coupling effect. Thus, it can be seen that the two controllers in the voltage loop can supplement each other.

According to Fig.6, the transfer function of voltage error $Verr(z)$ to periodic disturbance $d(z)$ is derived as

$$\frac{Verr(z)}{d(z)} = \frac{1-z^{-N}}{1+[S(z)P(z)-1]z^{-N}} = \frac{1-e^{-j\omega/f_r}}{1+[S(z)P(z)-1]e^{-j\omega/f_r}} \quad (10)$$

Where f_d, f_r and f_s are the frequency of periodic disturbance $d(z)$, the frequency of voltage reference V_{ref} and sampling frequency, respectively. Besides, $N = f_s / f_r$.

The angle frequency of periodic disturbance can be written as

$$\omega_d = 2\pi m f_r \quad (m = 0, 1, 2, \ldots) \quad (11)$$

According to Euler law, $Verr(z)/d(z) = 0$ .Under the steady state, zero steady-state error can be achieved by compensating waveform errors periodically. The tracking error $e(z)$ is expressed as

$$e(z) = e(z)[1-S(z)P(z)]z^{-N} + [(1-P(z))V_{ref}(z) + d(z)][1-z^{-N}] \quad (12)$$

From above equation, when $0 < |S(z)P(z)| \le 2$, the stability of designed repetitive controller can be ensured. The function of $S(z)$ can be designed as

$$S(z) = c \cdot z^{-k} \quad (13)$$

Where c is set to 0.5 , z^{-k} is a phase compensator allowing the reformed object to become a unity-gain in an expected frequency range. $k = \left[\frac{P_{Phase\ Delay}}{360/N}\right]$.

IV. SIMULATION

In order to simulate the proposed hybrid control scheme, the inductance variation simulation model should be built. Neglecting parasitical capacitance, the real filter inductor can be regarded as an ideal inductor in series with an inner resistor. The schematic diagram is shown in Fig.7. Where U is the voltage across the real inductor, V is the voltage across the ideal inductor, r is the real inductor inner resistor, i is the inductor current.

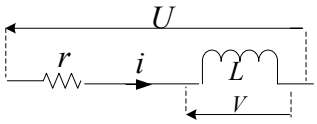

Fig.7 User-defined inductor module

The mathematic model of Fig.7 can be expressed as

$$V = U - r * i \quad (14)$$

Referring to Fig.5, a direct lookup table can be built to show the relation between the inductor current and real inductance. The accurate inductor simulation model is shown in Fig.8.

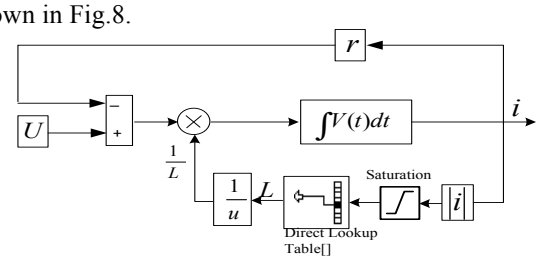

Fig.8 Inductance saturation characteristic simulation model

Computer simulation of the proposed dual buck inverter system controlled by the proposed hybrid control algorithm is implemented to study the output characteristics. A 2kW programmable AC power source was built for MATLAB digital simulation to verify the theoretical analysis. The main parameters of the system are as follows:

$L_1 = L_3 = 300\mu H$, $L_2 = 50\mu H$, $C = 5\mu F$, $r_1 = 50m\Omega$, $r_2 = 30m\Omega$, $V_{bus} = 210V$, $V_0 = 110V$, $f_s = 50kHz$. $c = 0.5$, $k = 3$. The simulation results are shown in Fig.9-12. In Fig.9 and Fig.10, blue represents the current waveforms of L_1, green represents waveforms of L_3 and red represents the waveforms of L_2.

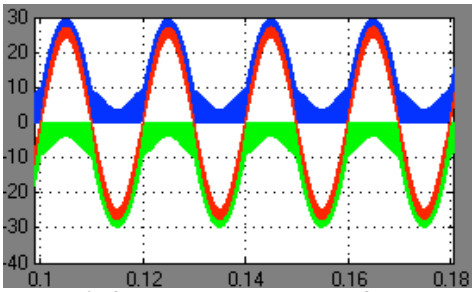

Fig.9 Inductor current waveforms

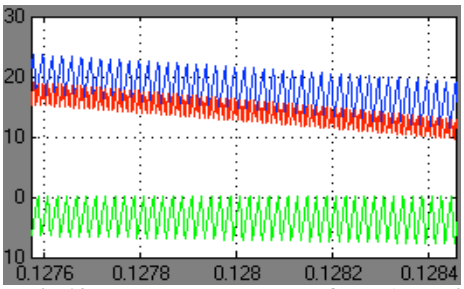

Fig.10 Inductor current waveforms(zoom in)

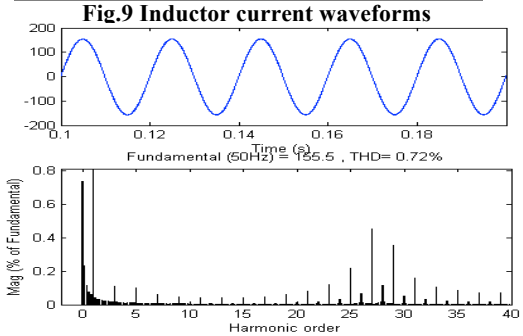

Fig.11 50Hz output spectrum at full rectifier load

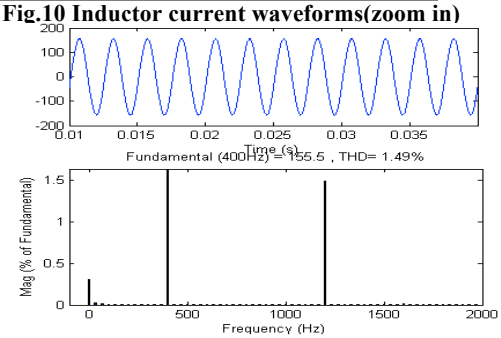

Fig.12 400Hz output spectrum at full rectifier load

It can be seen that the total harmonic distortion (THD) is 0.72% at 50Hz when the PACS is loaded with full rectifier load. The THD is 1.49% at 400Hz under the same loads. The designed PACS can provide the output waveforms with below THD 2.0%. Simulation results show that the theoretical analysis of the special switching sequence is true, and the hybrid controlled dual buck inverter for power stage of programmable AC power source can achieve high-quality output voltage waveforms.

V. CONCLUSIONS

In this paper, a modified dual buck half bridge inverter with three filter inductors adopting center symmetrical modulation mode has been introduced. In order to achieve lower THD and better dynamic response, a hybrid digital control scheme combining PID control with repetitive control as well as accurate deadbeat control has been presented for the closed loop voltage regulation of the dual buck inverter. The operating principle is simple and the approach can be efficiently implemented. The improved dual buck inverter and hybrid control scheme provide a foundation for future research on achieving a high-precision inverter. The simulation results from a 2kVA inverter for programmable AC Power Source verify the theoretical analysis of special switching sequence and hybrid control scheme.

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