Research on Design of a Management System for a Power Source Equalizing Charge based on FPGA Control

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***Abstract*—An accumulator can store energy in high capacity, and a super capacitor can charge and discharge high power. The mixed power source composed by an accumulator and a super capacitor can meet the high-power requirements of high capacity and peak value. How to perform equalized charging for multiple power packs is currently an emphasis in industry. On the basis of analysis for multiple equalizing charging methods, a new type of design scheme based on a DC/DC and a switch matrix is raised in this project. An intermittent charging mode was adopted, and four BCAP0350 served as the charging sample to perform the charging and discharging experiment as well as to verify the provided composite charging design scheme was feasible.**

***Index Terms*—DC/DC Type; Switch Matrix; Equalizing Charge; Intermittent charging; FPGA control**

I. INTRODUCTION

Electronic technical devices such as electronic instrument equipment, digital mobile terminals and electrodynamic force locomotives, especially for putting electronic equipment used for loading into operation, are being developed since they have characteristics such as high peak power and low average power. Namely, higher power output is required during peak value. Currently, the power density of an accumulator employed in the market is low, and the charging and discharging are slow. If meeting the demand of high current output is required, the accumulator must have high capacity, as this kind of power source may increase equipment loading. As a new type of energy storage element, the super capacitor has advantages [1] such as rapid charging and discharging, long service life, high power density, strong service environment adaptability, safety, and no toxicity. These advantages are very applicable for pulsatility loading; however, the energy density is low so the traditional accumulator cannot be replaced to individually supply power for loading. Currently, characteristics such as the high energy density of the accumulator and the high power density of super capacitor are combined to design a kind of mixed power source to improve the output power of the peak value and reduce the volume and mass of the power source for putting it into operation.

However, the rated voltage of a mixed power source for a single module is 3.2V so as not to meet the output demand of high-voltage equipment; therefore, this kind of mixed power source is required to conduct the series-parallel connection to meet the power supply demands of the equipment. The excessive charging and discharging of a monomer in the combined power source may shorten the service life of the power pack and even produce an explosion that threatens the equipment's safety. The primary cause for the excessive discharging of the monomer is the capacity difference in the power sources of each monomer inside the power pack. One of methods to solve this problem is the equalizing charge. This study's emphasis is on two parts: first, the design for equalizing the charge circuit topology and second, a study on equalizing the control strategy.

In regard to the design of equalizing charge circuit topology, the basis is whether the energy consumption may be divided into energy consumption type and non-energy consumption type. Therein, the energy consumption type is based on the resistance discharging equalizing method for heat dissipation and the energy consumption of the equalizing resistance; the non-energy consumption type is based on a switch capacitor method, a switch inductance method, a DC/DC method and a multi-winding transformer method [2]. Currently, there are problems such as long equalizing time and short universality for common equalizing method, so consistency based on the external pressure of the accumulator was adopted to judge the factor that the instability exists for equalizing. How to rapidly and effectively perform the equalizing charge for a single power source inside power pack is an important study direction in industry.

Beginning from the super capacitor in this project, the series connection of four mixed power sources served as the study object, and based on DC/DC and utilizing a switch matrix, the composite design thinking of a multi-equalizing charge was adopted to put forward the intersected charging design concept, design a power source management system, and establish the mathematical model for charging and discharging as well as design a kind of composite rapid charging method to demonstrate the feasibility of system existence via simulation and experimentation.

II. INTRODUCTION TO EQUALIZING CHARGE METHOD

As shown in Figure 1, the common equalizing charge method may be divide into an energy dissipation type and a non-energy dissipation type based on energy dissipation. Therein, equalizing with the energy dissipation type was to discharge the monomer accumulator with high capacity, respectively, through shunting the resistance in parallel on both ends of each monomer power source in the power pack and through shunting the resistance until the capacity

of all monomer accumulators was on same level. The design of this circuit is simple and the cost is low; however, the shunting resistance may be in working status and consume the energy of the monomer power source in the mode of heat [3] to be applicable with sufficient energy and generally good heat dissipation. The non-dissipation equalizing circuit was mainly studied in this project; the common non-energy dissipation equalizing circuit covers the following kinds:

A. Multi-winding transformer method

The principle of the multi-winding transformer method is shown in Figure 2; only a transformer is required for realization, with a convenient design and simple principle. The primary edge of the transformer is connected with input; each auxiliary edge is respectively connected with a charging receptor; in the design of the transformer, provided the number of turns of winding for each auxiliary edge is guaranteed to be same, the voltage of the auxiliary edge may be guaranteed to be same [4]. When unequalizing conditions occur for the monomer power source, Q breakover and the energy storage of the transformer are realized. After the QSTK cuts off, the energy is coupled onto the auxiliary edge. If the voltage of the power source monomer is lower than USTK/n, the power source monomer shall be connected with the diode of the monomer torque, the auxiliary edge of the transformer releases energy toward the monomer; the lower the terminal voltage, the more energy absorbed by the power source monomer. In the process of actual application, especially when there are more power source monomers required to be charged, the transformer structure may be more complex; meanwhile, the cost is higher for realization of complete consistency for winding the auxiliary edge. What is more, the mutual inductance matching among winding and the magnetic bias of the magnetic core for the transformer may cause instable charging and produce certain difficulties in application.

B. Switch Capacitor Method

Adjacent power source equilibrating type mainly means that the capacitor is the energy storage element that serves as the bridge of energy transfer to complete the energy equilibrium among each monomer power source inside the power pack. The principle is shown in Figure 3; each capacitor acts with two adjacent monomer power sources to convey the energy from a high-voltage monomer to a voltage monomer. Therein, Cf is the transferred capacitance, S1 and S2 are placed in Location 2, C2 may discharge toward Cf due to higher voltage, and the voltage for both becomes nearly equal. The above-described action is conducted many times to realize the transfer of electric energy on C1 and C2 to reach the purpose of voltage equilibrating [5] .The insufficiency of this kind of scheme is because the slow equilibrium speed, complex circuit and characteristics of a multi-way switch cannot appropriately enable the complete equilibrium between two monomer power sources. On the other hand, an individual circuit parameter is required for configuration of different power source systems, the parameter selection is difficult, and the research and development are difficult. The capacitor is utilized to transfer the energy, and the inductance is also utilized to transfer the energy. Further introduction will not be conducted due to limit of paper length.

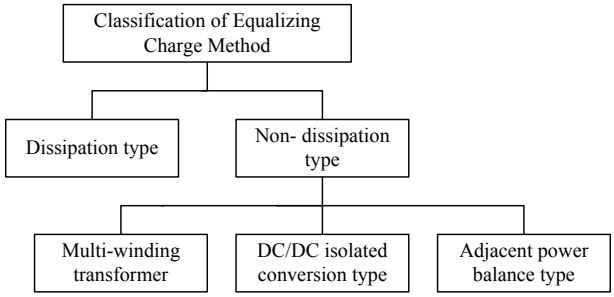

Figure 1. Category on Common Equalizing Charge Method Currently

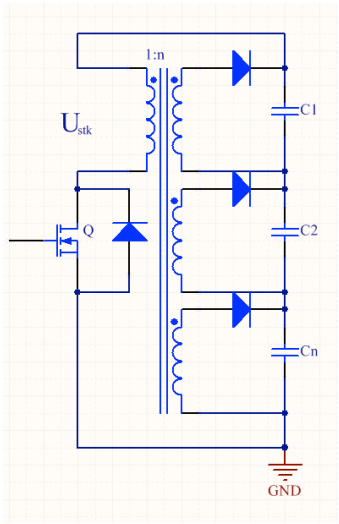

Figure 2. Schematic Diagram of Multi-winding Transformer Method

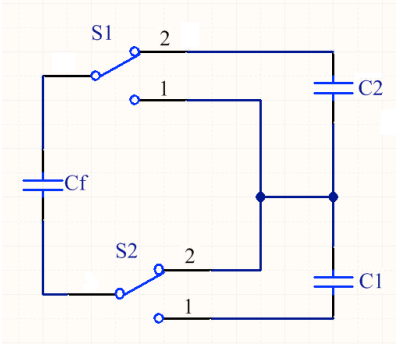

Figure 3. Principle Diagram of Switch Capacitor Method

C. Charging Method with Series-Parallel Conversion for Switch Matrix

The principle of this method is shown in Figure 4, indicating that multiple power source monomers in series convert as a parallel form via a switch matrix while charging to simultaneously guarantees an individual charge for each power source body. The series form is charged after completing the charging to be used for the discharging. While charging, we closed S1and S2 as well as opened S3 to enable monomer power sources C1 and C2 to work under parallel status. After completing the charging, we disconnected S1 and S2 as well as closed S3 to enable monomer power sources C1 and C2 to work under series status. The principle structure for this kind of method is simple for realizing the deep charging and discharging; however, in the actual application, electrotechnics difficul-

ty exists, only being applicable for the condition that the number for monomer power sources in series is less. When the number for monomer power sources in series is more, the quantity of switches is extremely large and the wiring may be very complicated.

D. DC/DC Method

The DC/DC convertor was adopted with the power tube as the connection between the front end and back end, via digital control, to achieve control of the DC voltage in the back end by controlling the breaking time of the power tube with a "chopping" signal. The item was taken with FPGA as the main control chip to monitor the voltage, current, and other signals in real time and adjust the duty ratio to output stable DC voltage according to the monitoring value. The DC/DC convertor is usually divided into boost, buck and boost-buck according to its function. We studied and discussed the boost-buck DC/DC convertor [6].

The schematic diagram of the boost-buck circuit is shown in Figure 5, which not only can be used as a step-down circuit but also can be used as a boosted circuit. Among them, L is the inductance, D is a one-way connected diode, C is the capacitance, and T is a power tube. When the control end of T is input with the full impulse voltage, T is forward connected and cut off when it is zero. At the stage of connecting the power tube, the input current returns after passing T and L due to the existence of D. At this moment VL=Vi and the current of inductance is increasing step by step. At the moment of t1, T is switched off, input voltage Vi and the back end are switched off, the current of L returns through D after passing the load, and at the same time, the current of capacitor C returns to the negative terminal through the load. The current of inductance gradually decreases, and the voltage is in the opposite direction, with the inductance as the energy source, this moment of inductance voltage VL=Vo.

At the stage of connecting the power tube, inductance current:

$$i_L = \frac{\int_0^{t_1} V_L dt}{L} = \frac{\int_0^{t_1} V_i dt}{L} = \frac{V_i \times t_1}{L}$$

In Switching off the power tube, inductance current:

$$i_L = \frac{\int_{t_1}^{T} V_L dt}{L} = \frac{\int_{t_1}^{T} V_o dt}{L} = \frac{V_o \times (T - t_1)}{L}$$

According to current balance principle:

$$\frac{V_O}{V_{in}} = \frac{t_1}{T - t_1} = \frac{D}{1 - D}$$

Among them $D = t_1 / T$ is the duty ratio.

The above formulas show the specific value of input voltage and output voltage can be adjusted by the duty ratio of input square wave to achieve the constancy of the output voltage by controlling the square wave inputting of the control end of the DC/DC circuit according to the change of the input voltage.

The principle of the charging method of DC/DC is shown in Figure 6, which is constant-voltage charged by

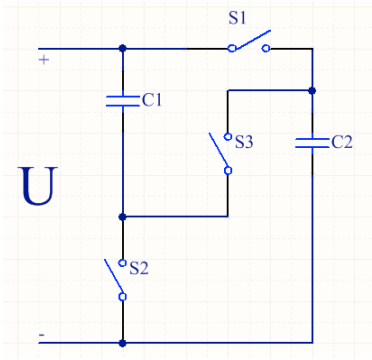

Figure 4. Charging Method with Series-Parallel Conversion

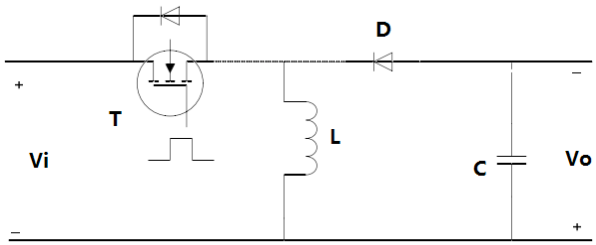

Figure 5. Schematic Diagram of Boost-Buck DC/DC Convertor

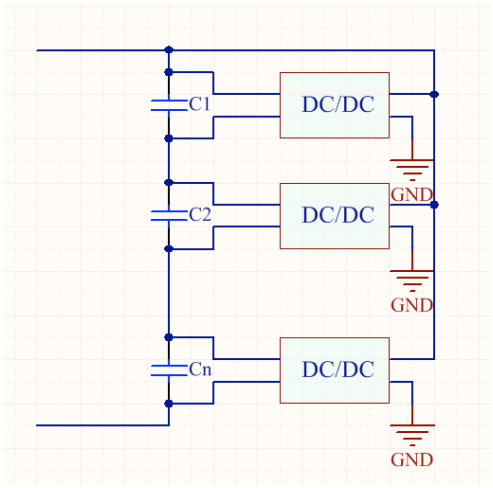

Figure 6. Block Diagram for Charging Principle of DC/DC

the parallel charging monomer of the DC/DC module, when the voltage of the power source monomer is lower than the rated value. The DC/DC module will charge it. When the voltage value reaches the rated voltage, we closed the DC/DC module. The system power source can charge several power source monomers at the same time by this method, with high accuracy, small consumption, and high charging speed, but the DC/DC module must be matched with the power source monomers one by one; when the power source is made up of several monomers, the overall charged circuit system will be very large, complex, and the cost will be very high [7].

III. A MODIFIED NEW AND EQUALIZING CHARGING CIRCUIT DESIGN

Compared with the above equalizing charging circuits and in view of their advantages, a new and equalizing charging circuit with FPGA as the core, based on the

switch matrix and DC/DC module, was designed; this circuit is only adopted with one DC/DC module and is charged circularly by the switch matrix. Using only one DC/DC module guarantees accuracy of the equalizing charging; meanwhile the circuit cost is reduced. But this method is limited by the work of the switch matrix and is not suitable for excessive capacitor charging. If charging of several super-capacitors is required, they can be grouped to use this method, and the parallel mode will be used to carry out equalizing charging between the groups.

The system principle is shown in Figure 7, which is composed of the charging module (on the left) and the monitoring module (on the right). The specific work procedure of the system is as follows: the FPGA carries out waveform control to the DC/DC module. To output the power source of each monomer to charge after voltage transformation, the charging target was selected by the FPGA controlling switch matrix. The switch matrixes consist of SW1, SW2, SW3, SW4, a single blade four set switch and a single blade switch SW5. When charged, we switched off the SW5 first, and when the four single blade four set switches were at a position of "1", the DC/DC module charged monomer power source 1. Similarly, the monomer power sources 2, 3, 4 could be charged, respectively. After completion of charging, the four single blade four set switches were switched off and SW5 was closed. The FPGA monitored the charging current in real time by the AD1 and controlled the DC/DC module and switching network based on the sampling value. In the process of charging, the system monitored the voltage of the power source monomer in real time, and the monitoring value coupled the data to the AD2 by an optocoupler and was sent to the FPGA for analysis after being sampled and to the control the switch matrix, to charge modules 1, 2, 3, 4 of monomer power source, respectively [8].

IV. IMPROVEMENT OF WAY OF INTERRUPTING METHOD CHARGING IN VIEW OF SUPER CAPACITOR

The traditional charging methods are frequently adopted with a two stage charging style of "the constant electric current and the constant voltage." This method can avoid the impact of the peak current to the monomer power source and the DC/DC circuit for protection of the equipment. The constant current mode is used in the first stage. The voltage of the single power source increases gradually with time, and when the voltage of the single power source reaches a certain value, it changes over to constant voltage mode and the charging current is reduced gradually until is fully charged. This item carries out segment treatment for the first stage charging process, to use an

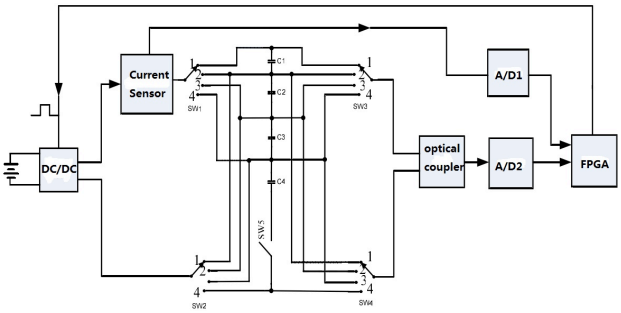

Figure 7. Block Diagram of Combined Type Equalizing Charging Design Principle

interrupted method to charge, which not only protects the super capacitor in the single power source, but also causes no obvious effect on charging time. The specific working principle is shown below: the FPGA samples the system voltage and current by A/D, and when the current value is too big, the FPGA chip will close the control end of the DC/DC module for several periods. At this moment the DC/D module is in the state of not working, the charging current reduces rapidly, the single voltage value of the super capacitor does not increase, and the FPGA chip opens the switch and continues to control the PWM end. Thus the charging current can be maintained as constant. After the voltage of the power source monomer is increased to a certain value, the charging mode is changed to constant-voltage charging, that is to fix the square wave duty ratio of the PWM control end of the DC/DC module until the single power source is charged to the rated voltage to complete the charging of the power source monomer, and then it is switched over to the position of the switch, charging the next power module [8].

According to the charging methods, the control procedure of the FPGA is shown in Figure 8. When starting the system, all the switches were placed at the position of "1" to conduct charging control to the super capacitor C1, and the PWM end of the DC/DC circuit was adopted with a waveform with duty ratio D=d to charge. When the charging current was too big, we closed the PWM end, this moment is D=0 and the charging current is reducing. When charging current I is reducing below the required current, we opened the control of the PWM end to continue to carry out the D=d charging mode until the voltage value of super capacitor C1 was charged to the required value, and then charged with the constant voltage method: that is D was a fixed value, charged to the rated voltage and then switched over to the next super capacitor monomer, round-robin like this, and finally finished the equalized charging of the whole super capacitor unit.

TABLE I.
MEASURING VALUE OF CHARGING RESULT

	I	II	III	IV	V	VI	VII	VIII	IX	X
C1	2.68	2.69	2.73	2.73	2.76	2.71	2.71	2.69	2.72	2.68
C2	2.71	2.72	2.72	2.72	2.69	2.73	2.70	2.71	2.71	2.70
C3	2.69	2.72	2.71	2.68	2.72	2.70	2.70	2.69	2.68	2.69
C4	2.75	2.74	2.77	2.73	2.73	2.75	2.74	2.73	2.69	2.71
Capacity Deviation	0.07	0.05	0.06	0.05	0.07	0.05	0.04	0.04	0.04	0.03
	97.4%	98.2%	97.8%	98.2%	97.5%	98.2%	98.5%	98.5%	98.5%	98.9%

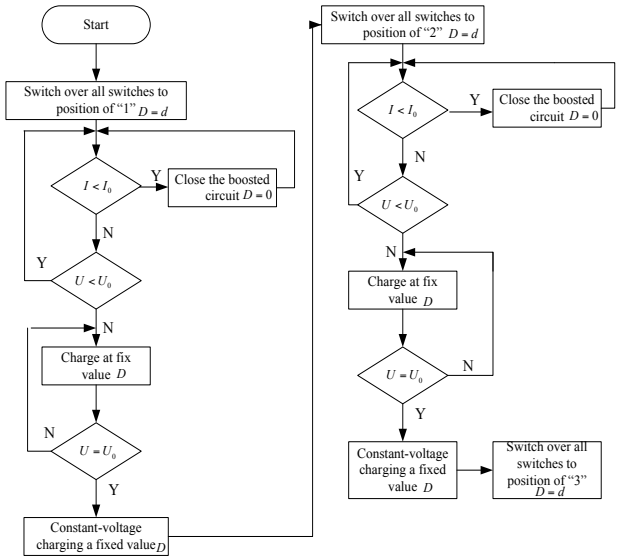

Figure 8. FPGA Control Flow Diagram

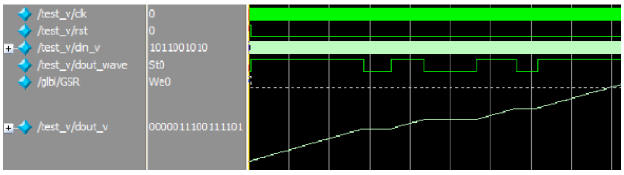

Figure 9. Simulation Effect of Disconnected Charging

V. CONCLUSION

This project is combined with several mature equalizing charging methods to put forward an equalizing charging design based on a switch matrix and DC/DC module and to set up the related model and real system according to the design thought. The charging process was adopted with a disconnected charging method to guarantee the work of the super capacitor within the rated current. The simulation of the charging process is shown in Figure 9.

The project used four BCAP0350 super capacitors by Maxwell as the charging monomer samples; the rated voltage was 2.7V, and the rated capacity was 350F. Using this method to charge, after completion of balancing, the voltage values of the four capacitor monomers are as shown in Table I, the maximum error of the monomer in the same group is 0.07V, and the purpose of equalizing charging is reached.

It was observed from the simulation and validation results of this project that the DC/DC + switch matrix mode was used to reduce the DC conversion module and to increase the switch matrix network. When the number of power monomers in a power group is increased, the cost of the complexity of the switch matrix will increase. The system design method set forth can be applied in the work environment with few monomers. In the case of a large number of monomers, multiple group paralleling can be used. How to balance the charging time of the monomers in the group and the number of monomers being grouped is the research direction of the next stage.

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