Design of High-precision Broadband Closed-loop Driving Power on Dielectrophoresis

http://dx.doi.org/10.3991/ijoe.v12i06.5513

Keqiang Dong, Qihua Yang
China Jiliang University, Hangzhou, China

***Abstract*—With the development and application of Biological chips and sensors, the demand for high-precision broadband driving power is increasingly rigorous. In order to improve the precision and reliability of the driving power, a high precision broadband closed-loop signal generator has been designed. It works by the high-accuracy amplitude detection circuit, the broadband voltage controlled amplifier and a micro-controller. The principles of amplitude detection circuit and amplifier circuit have been elaborated. Within 1 MHz ~ 200 MHz band, within 1 ~ 10 VPP amplitude range, under 50 Ω output impedance, the error of output signal amplitude can be controlled effectively. Precision is up to 0.15%. It meets the index and scientific research's requirement.**

***Index Terms*—Amplitude detection, Broadband, High precision, Impedance matching**

I. INTRODUCTION

With the development and application of Biological chips and sensors, the demand for high-precision broadband driving power is increasingly rigorous. Especially in the biological electrophoresis experiment, the precision and stability influence the tests' success directly. It also has relationship to the development and progress of biotechnology [1-4]. However, the existed high-precision driving powers have narrow band, and the broadband are not accurate enough [5-7]. Therefore, the design of high-precision, broadband, closed-loop driving power system is proposed. It mainly consists of AD9953, DDS (Direct Digital Synthesis) chip, high-precision amplitude detection circuit, broadband voltage controlled amplifier and STM32 microcontroller.

According to the experimental requirements, the design index shows as follow: ①The output frequency ranges from 1 MHz to 200 MHz; ②The peak-to-peak output voltage amplitude ranges from 1V to 10V, and the absolute amplitude error is less than 3 mV; ③Output impedance matches 50 Ω.

II. SYSTEM DESIGN OF DRIVING POWER

Driving power system block diagram is shown in figure 1. Input data are translated into frequency words and amplitude words by STM32. Then the words are transferred to AD9953 to generate the corresponding original signal. After that, the signal outputs by low-pass filter, voltage-controlled amplifier and secondary amplifier. Output signal gets feedback to input port through amplitude detection circuit. At last, it realizes the amplitude error correction by changing the voltage controlled amplifier's gain.

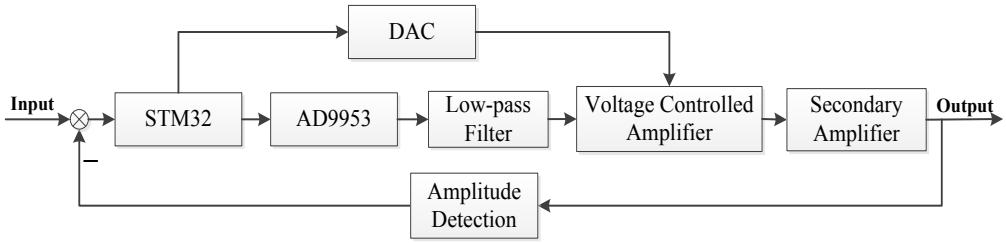

Figure 1. System block diagram

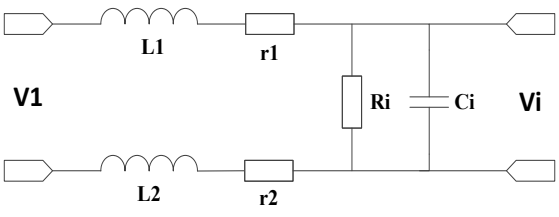

Figure 2. Input equivalent circuit

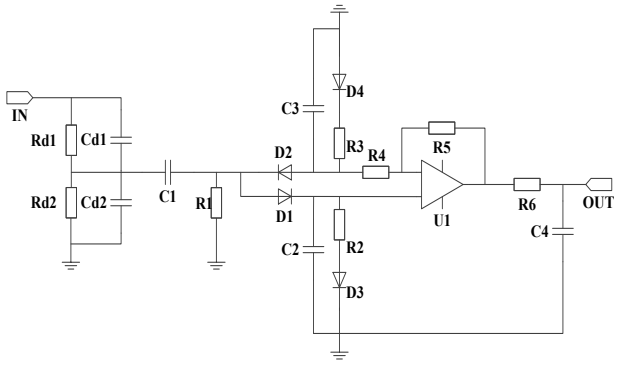

Figure 3. Bleeder detection circuit

III. DESIGN OF HIGH-PRECISION AMPLITUDE DETECTION CIRCUIT

Amplitude detection circuit consists of bleeder detection circuit and high-precision ADC (Analog-to-Digital Converter). It makes output voltage signal which is the high frequency sine wave signal to be proportional DC voltage signal by the bleeder detection circuit. And then, measure it by high-precision ADC.

In the detection circuit design, natural resonant frequency has to be considered to make sure the accuracy of measurement [9]. Figure 2 shows the input stage equivalent circuit in detection circuit. L_1, L_2 mean the conductor inductance. And r_1, r_2 mean the lead resistance. C_i means input capacitance, R_i means input resistance, V_1 means the test voltage signal, V_i means input stage output signal.

The input stage's natural resonant frequency f_φ is:

$$f_\varphi = \frac{1}{2\pi\sqrt{L_i C_i}} \quad (1)$$

If the test voltage frequency $f = f_\varphi$, V_i will be V_1's Q times:

$$V_i = Q \times V_1 \quad (2)$$

Q means quality factor of the input stage, the ratio of reactance and capacitance。

Therefore, input stage's natural resonant frequency should be many times higher than the test signal frequency, otherwise serious measurement error will exist. In the design, take $Q \geq 10$ and the test signal frequency to 200 MHz.

Bleeder detection circuit is shown in figure 3. It applies the modified temperature compensation double balance peak detection diode structure [10]. The structure can effectively eliminate the thermal effect in different metal connecting and suppress harmonic errors. Simultaneously, it could improve the signal-to-noise ratio in the small signal measurement. Detector diode D_1 and D_2 choose IN60. Bleeder circuit consists of high frequency non-inductive precise resistance R_{d1}, R_{d2} and high frequency non-inductive precise capacitance C_{d1}, C_{d2}. The ratio of bleeder is set to 1:1. The capacitances and resistances in the design strictly choose high-frequency non-inductive high-precision capacitances and resistances and U_1 choose ultra low noise operational amplifier.

The detector diode voltage signal is made up of DC bias voltage and small AC voltage signal, can be represented as:

$$V(t) = V + v_0 \times \cos(w_0 t) \quad (3)$$

The current though the detector diode:

$$\begin{aligned} I &= I_0 + v_0 G_d \cos w_0 t + \frac{v_0^2}{2} G_d' \cos^2 w_0 t + \cdots \\ &= I_0 + \frac{v_0^2}{4} G_d' + v_0 G_d \cos w_0 t + \frac{v_0^2}{4} G_d' \cos 2 w_0 t + \cdots \end{aligned} \quad (4)$$

I_0 means bias current, G_d means diode dynamic admittance:

$$G_d = \frac{dI(v)}{dV} | v_0 \quad (5)$$

The output differential voltage signal by detector diode:

$$V_o = (1 + \frac{R_5}{R_4}) V_{IN+} - \frac{R_5}{R_4} V_{IN-} \quad (6)$$

V_{IN+} means the output of D_1, V_{IN-} means the output of D_2.

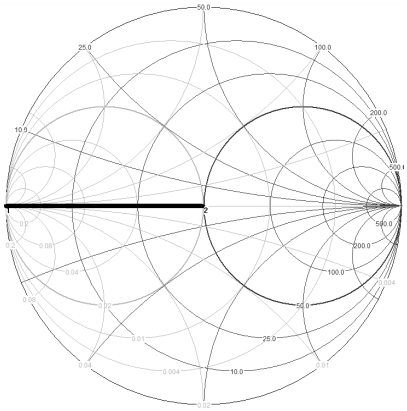

Figure 4. Smith impedance chart

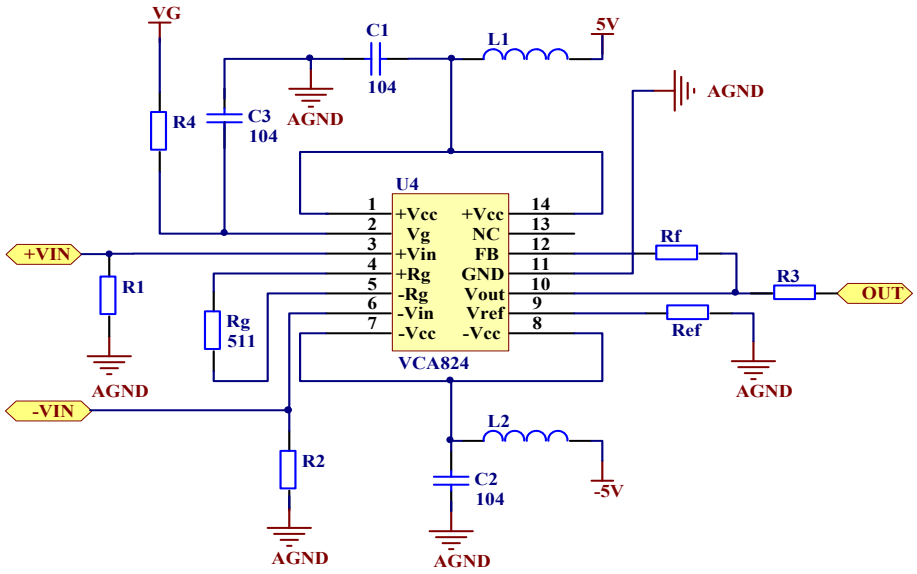

Figure 5. Voltage controlled amplifying circuit

High-precision ADC module uses ADS1220, the 24-bit ADC chip as the core. Set 15V as the full range. Measure ENOB (Effective Numbers of Bits) by noise testing method: Empty the input ports. Convert the noise to calculate the effective digits.

If N data have been gathered and the data x_i correspond to sequence number i, the average $\overline{X}$ can be represented as:

$$\overline{X} = \frac{1}{2}\sum_{i=1}^{N} x_i \quad (7)$$

Standard deviation S represented as:

$$S = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(x_i - \overline{X}\right)^2} \quad (8)$$

ENOB represented as:

$$ENOB = 24 - (\log_2 S + 1) \quad (9)$$

By the test, in the 20th SPS (Sample Per Second), ENOB is 19.48 at least. Set it as 19 in design.

IV. DESIGN OF AMPLIFIER CIRCUIT

Because working frequency band overlaps the radio frequency band partly, it is necessary to consider the impedance matching and electromagnetic interference problems. Refer to VCA824 datasheet [11]. Set working frequency as 200 MHZ. Amplifier's input and output impedance calculated as follows:

$$Z_{in} = 6.33\times10^{-25} - \left(7.96\times10^{-10}\right)\times j \quad (10)$$

$$Z_{out} = 0.01 - 0\times j \quad (11)$$

Match impedance by Smith impedance chart shown in figure 4. Then we can get the schematic circuit diagram of voltage controlled amplifier as shown in figure 5.

The voltage controlled gain V_G connects DAC7631, 16-bit DAC. V_G ranges from -1 V to + 1V, ENOB is 14 digits. In theory, the minimum resolution is 0.13 mV, actually set 3 mV. Set the largest magnification of VCA824 as 6 times. The theoretical minimum controllable magnification is 0.01 times.

In order to meet the voltage amplitude of design index, the secondary amplifier is required. The maximum output voltage signal from DDS is 500 mV. In order to ensure the signal do not distort, the maximum output of VCA824 is set 2 V. Therefore, the secondary amplifier's minimum magnification must be 5 V/V at least. Actually, it is 6 times to prevent accidents. Choose two THS3091 parallel operation ways to improve the output current [12]. Set the working frequency as 200 MHz, amplifier's input and output impedance calculated as follows:

$$Z_{in} = 2.44\times10^{-23} - \left(3.98\times10^{-9}\right)\times j \quad (12)$$

$$Z_{out} = 0.03 - 0\times j \quad (13)$$

By the formula (12) and (13), the secondary amplifier's Smith chart is similar to figure 6.

V. SOFTWARE DESIGN

System software process is shown in figure 6. The system starts and initializes at first. Then user goes to set the output amplitude and frequency. System judges whether the input data overflow. If they do, ask to input again, or update the frequency and amplitude control words in turn. The frequency words control AD9953 output frequency, the DDS amplitude words control AD9953 output amplitude. Both of them update once each input. Voltage-controlled amplitude words control Vg port's amplitude (-1V ~ 1V) of VCA824. It updates thrice per second when the output error is greater than 0.15%.

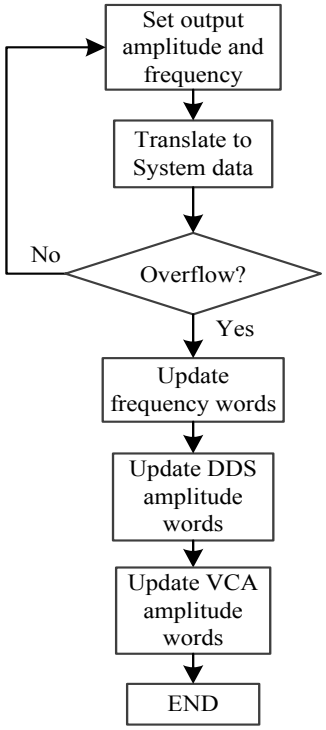

Figure 6. The system software process

Control algorithm of DDS frequency:

$$f_{OUT} = \frac{(FTW)(f_S)}{2^{32}} \quad (14)$$

f_S represents system clock frequency. FTW mean frequency control words $\left(0 \le FTW \le 2^{31}\right)$, 2^{32} means the capacity of phase accumulator.

Control algorithm of DDS amplitude:

$$A = \frac{ACR}{2^{14}} V_{\max} \quad (15)$$

$V_{\max}$ represents the maximum output voltage amplitude of DDS. ACR means amplitude control words.

In order to improve the efficiency of the closed loop correction, measure the relationship between the control voltage and the voltage controlled amplifier's gain in different frequencies. And store it in STM32 by tables. When test data are more than the stored data, calculate by function as follow:

$$A = \left(2.9771\times V_G + 3\right)\times C \quad (16)$$

A (V/V) represents amplifier magnification, V_G means control voltage($-1V < V_G < +1V$), C means Frequency correction constant, measured by test.

VI. SIMULATION AND EXPERIMENTAL TEST

The capacitance and resistance in actual circuit are high-precision and non-inductive. The accuracy could reach 0.1%. Correct random error in the production by software.

Driving power system simulation mainly uses ADS2011 in high frequency band (10M ~ 200M). Provide a reference for PCB layout and actual wiring by the board level high frequency structure simulation.

Measure the debugged driving power system by ultra high-frequency digital-display millivoltmeter THS2281 and frequency meter Agilent E1420BVXI. The results are shown in table 1 and table 2.

TABLE I. THE FREQUENCY TEST RESULTS

Set value (MHz)	Measure value(MHz)	Relative error(%)
1	1.00002	0.002%
10	10.00031	0.0031%
50	50.00232	0.0046%
100	100.01062	0.0106%
150	150.03101	0.0207%
200	200.04621	0.0231%

TABLE II. THE AMPLITUDE TEST RESULTS

Set value (V)	Measure value(V)	Relative error (%)
1	1.001	0.100%
2	2.002	0.100%
3	3.002	0.067%
5	4.998	0.040%
10	10.003	0.030%

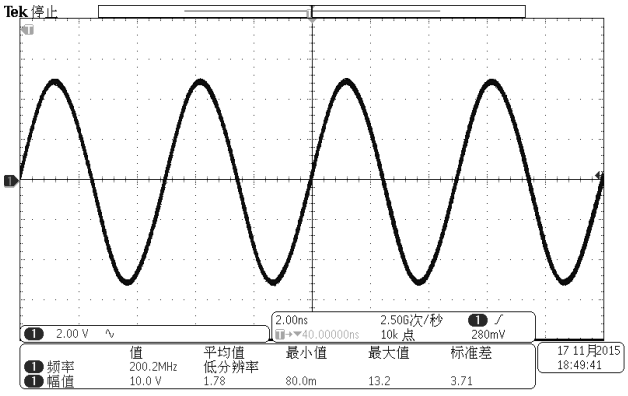

Figure 7. The waveform with 50Ω

Figure 7 is the output waveform with 200 MHZ, 10 V, 50 Ω load.

VII. CONCLUSION

The design of high-precision, broadband, closed-loop driving power system on dielectrophoresis is proposed. It mainly consists of AD9953, high-precision amplitude detection circuit, broadband voltage controlled amplifier and STM32 microcontroller. From the experimental results, the output frequency and amplitude reach the design index. The waveform on load is satisfactory. The maximum relative error of output amplitude is less than 0.15%. The absolute error is less than 3 mV. It meets the design index and scientific research's requirement.

REFERENCES

[1] Khashayar K, Saeid N, Sara B, et al., "Dielectrophoretic platforms for bio-microfluidic systems," Biosensors and Bioelectronics, vol.26, pp.1800-1814, 2011 http://dx.doi.org/10.1016/j.bios.2010.09.022

[2] Odorizzi L, Ress C, Collini C, et al., "An integrated platform for in vitro single-site cell electroporation: controlled delivery and electrodes functionalization," Sensors and Actuators B: Chemical, vol.170, pp.182-188, 2012 http://dx.doi.org/10.1016/j.snb.2011.06.027

[3] Isabella G, Xiong C Y, Fang J, "Low-voltage electroporation with fluidic microelectrodes," Microelectronic Engineering, vol.98, pp.707-710, 2012 http://dx.doi.org/10.1016/j.mee.2012.05.026

[4] Fernanda C A, Lin G, Alexandra R, "Transitioning streaming to trapping in DC insulator-based dielectrophoresis for biomolecules," Sensors and Actuators B: Chemical, vol.173, pp.668-675, 2012 http://dx.doi.org/10.1016/j.snb.2012.07.080

[5] Wang Yi, Xie Qi, Lv Ting, Gu Qimin, "Design and Realization of High Accuracy and Multi-channels Synchronous Sinusoid Signal Generator," Computer Measurement & Control, vol.11, pp.2663-2665, 2010

[6] Liu Lei. "Design of a DDS-based Signal Source and Research on the Relevant Key Technologies," M.S. thesis, Dept.Electron., China, Nanjing University of Science and Technology, Nanjing, China, 2013.

[7] Bao Lixing, Chen Xiaozheng, "Design of A High Accurate Signal Generator," Computer Measurement & Control, vol.4, pp.588-590, 2008,

[8] Analog Devices. (2015, March 10).400MSPS 14-Bit 1.8V CMOS Direct Digital Synthesizer [Online]. Available: http://www.analog.com.

[9] Ruan Bin, "Design and Realization of High Frequency Voltage Standard Device," M.S. thesis, Dept.Electron., China, Engineering University, Harbin, China, 2012.

[10] Xiong Lan, Qihua Yang, Ke Zhang. "Design of wide-bind and multi-channel synchronous output driving power on dielectrophoresis," the 3th International Conference on Civil Engineering, Architecture and Building Materials, Jinan, CEABM ,2013, pp. 1056-1059.

[11] Texas Instruments. (2015, April 23) Ultra-Wideband >40dB Gain Adjust Range Linear in V/V Variable Gain Amplifier [Online]. Available: http://www.ti.com.

[12] Texas Instruments. (2015, April 23) High-Voltage Low-Distortion Current-Feedback Operational Amplifiers [Online]. Available: http://www.ti.com.

AUTHORS

Keqiang Dong is with College of Quality & Safety Engineering, Key Laboratory of Furniture Inspection Technology of Zhejiang Province, China Jiliang University, Hangzhou, China. He is now a Current Master Student engaged in embedded hardware and software system development (e-mail: rafael723235@163.com).

Qihua Yang is with College of Quality & Safety Engineering, Key Laboratory of Furniture Inspection Technology of Zhejiang Province, China Jiliang University, Hangzhou, China. He is now a professor engaged in detection technology and automatic equipment (e-mail: 000066@cjlu.edu.cn).

Submitted, 24 January 2016. Published as resubmitted by the authors on 08 May 2016.