Design and Implementation of Time Synchronization Experimental System for Wireless Sensor Networks

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Abstract—Time synchronization is a basic requirement for various applications in wireless sensor network, such as target tracking, event detection, speed estimation and sensor nodes cooperation. The basic principle of the reference broadcast synchronization protocol using in wireless sensor networks is present, and a compact reference broadcast synchronization experimental system is designed and implemented in this paper. The experimental results show that the receivers of the system can successfully capture the timing packets issued by the broadcast beacon within 200 meters and simultaneously adjust their local clocks according the timing packets. The time synchronization error between the receivers is less than 410 microseconds. The circuit design scheme of the time synchronization experimental system proposed in this paper may be taken as technical reference for the planning and designing of low cost, miniaturization and high accuracy nodes in wireless sensor networks.

Keywords—wireless sensor networks, sensor node, time synchronization, reference broadcast synchronization, broadcast beacon

1 Introduction

In a wireless sensor networks, due to the cost constraint, the sensor node usually has unfavorable clock precision. Over time, the time difference between the node clocks will become bigger and bigger, and this problem would become more and more serious along with the growth of the sensor node number in the wireless sensor networks. However, many important basic functions of wireless sensor networks, such as detection, location, velocity estimation and so on, require the sensor nodes to maintain relatively uniform timescale. So nowadays, the problem of time synchronization in wireless sensor networks is getting more and more attention [1-3].

In the past few decades, many time synchronization protocols or methods for wireless sensor networks have been designed [4-6]. For example, some people introduce the Internet's time synchronization protocol standard NTP (Network Time Protocol) into the wireless sensor networks. The NTP mainly uses time deviation and delay estimation methods to synchronize the clocks on the internet platform. It contains a hierarchical tree structure formed by time servers, and the root server at the bottom is usually synchronized with the UTC (Universal Time Coordinated). Similar to NTP, some other wireless communication protocols adopt GPS (Global Positioning System) as their standard time, in order to bring about the clock synchronization [7-9]. However, these methods are not suitable for wireless sensor networks, because there is a lot of energy needed to maintain consistency with the world time standard. Wireless sensor networks are usually limited to size, power, and complexity, and the sensors in network do not have enough energy to apply this kind of methods. The more popular timing protocols currently in use for wireless networks are Timing-sync Protocol for Sensor Networks (TPSN) and Flooding Time Synchronization Protocol (FTSP) [10-12].

TPSN is the extension of the NTP protocol to adapt to the application of wireless sensor networks. And simply stated, TPSN is a sender to receiver synchronization. The implementation of this protocol is usually divided into two phases: the level discovery phase and the synchronization phase. In the first phase, a node clock is selected for the entire network as a reference time, and then this node is set as a root node. Ultimately, the entire network is arranged into a hierarchical spanning tree structure based on the root node. In the following synchronization phase, along the branch tree structure, every node has to shake hands with their parent nodes in order to achieve information transmission. And then the difference between the local clock time is corrected and compensated, and the final clock synchronization is realized. Both phases are initiated from the root node. FTSP is another sender to receiver synchronization protocol. FTSP broadcasts it timing information to all nodes within the broadcast range. Then those nodes calculate their time offset from the global time successively. The receiving nodes usually calculate their time different using linear regression. In addition to TPSN and FTSP, several other time synchronization methods have been mentioned in reference [12], such as Time Diffusion Synchronization Protocol (TDP), Consensus Clock Synchronization (CCS) and Clustered Based Consensus Time Synchronization Algorithm (CCTS). The advantage of TDP is that the performance of voice and video applications can be improved when multiple sources are sending data back to the sink through directed diffusion. CCS provides the internal synchronization for the vertual clocks. This algorithm is fully decentralized and robust for node failures and mobility and there is no requirement for a reference clock. CCTS improves the convergence rate due to the combination of clustering topologies and reduces the communication traffic in comparision to distributed consensus algorithm. Reference Broadcast Synchronization (RBS) is another more popular timing protocol currently in use for wireless networks. But RBS is different from most of these protocols mentioned above because it uses receiver to receiver synchronization [13-14].

This paper devotes to the study of RBS protocol used in wireless sensor networks and the development of a RBS time synchronization experimental system. The structure of the paper is organized as follows: Section 2 presents the basic principle of the RBS protocol, describes the typical form of a RBS system and compares the RBS system with the traditional synchronization system. Section 3 gives the design of a RBS time synchronization experimental system. Section 4 expounds in detail the experimental design, experimental sequence and experimental result. Finally, Section 5 concludes the paper.

2 Principle of reference broadcast synchronization

The main idea of RBS is that a designated root node would broadcast a beacon to all the other nodes. Multiple nodes would receive the beacon simultaneously and note their local time upon reception. And these receivers can also compare their clocks to one another to calculate their relative phase offsets. A most simple RBS system is usually made up of one broadcast beacon and two receivers. Two receivers will regularly receive timing packets issued by the broadcast beacon and will adjust their local clocks in time according to the received timing packets.

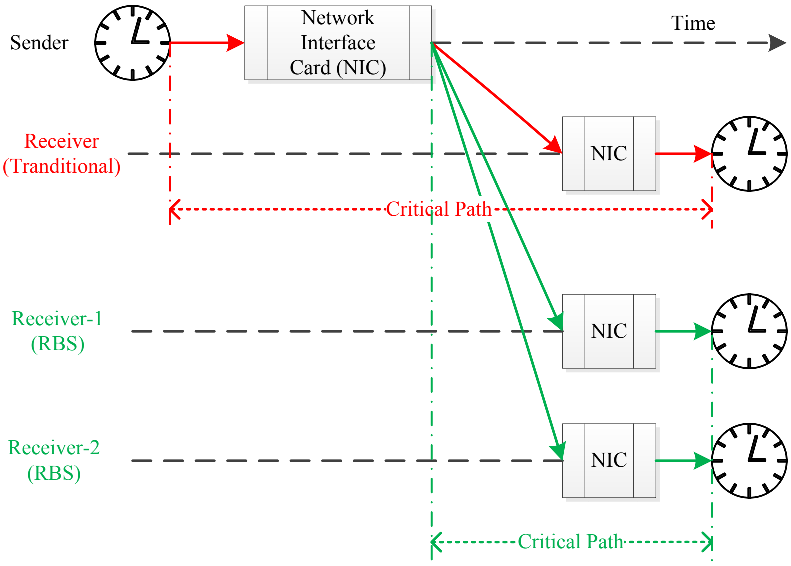


Fig. 1. Comparison of a traditional synchronization system with RBS

The main advantage of RBS is that this protocol can eliminate the uncertainty of the sender by removing the sender from the critical path. In one-to-all broadcast, a critical path of a network is the longest path among the shortest ones from the source node to other nodes in the network. Nodes in a critical path are referred as critical nodes. Just as the top diagram shown in Fig.1, the critical path in the traditional system includes the sender. But in the RBS, the critical path only contains the propagation and receive time uncertainty. It is because of that RBS is a receiver to receiver synchronization method, and different from the traditional sender to receiver methods. When the transmission range is not big, the propagating time is negligible. It can be considered that the reference beacon could arrive at all the receiving nodes instantaneously. Then it can come to the conclusion that the only room for error is the receiver uncertainty.

One broadcast and two receivers forms the simplest structure of a RBS system. It can be expanded to synchronization between N receivers, where N is greater than two. In this case, more than one broadcast would be required, because of that the more the number of broadcast the higher the synchronization accuracy.

3 Design and implementation of RBS experimental system

In order to verify the validity and feasibility of the RBS protocol, an experimental system has been designed and implemented. In the experimental system, the RBS synchronization process is initiated by the broadcast beacon.The broadcast beacon will broadcast a time_sync packet at time T_0 to the receivers.The time_sync packet cacontains a pulse-per-second signal's logic level ("0" or "1") retained by the broadcast beacon and the time T_0 when it was sent. These receivers will receive and disassemble the time_sync packets periodically, and fine tune their local clocks acorrding to the received time_sync packet, as well as produce and maintain their own pulse-per-second signal.

Beacause the most simple RBS system is usually made up of one broadcast beacon and two receivers, so three nodes have been developed, including one sender and two receivers. Both of the sender and receiver include a power circuit, a wireless communication circuit and a microcontroller. Fig.2 gives the brief design scheme of the node in the RBS time synchronization experimental system.

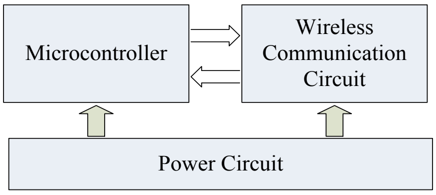


Fig. 2. Scheme of System

The power circuit is designed based on AMS1117-3.3, just as shown in Fig.3. AMS1117-3.3 is a low dropout voltage regulator produced by Advanced Monolithic Systems, Inc. The AMS1117-3.3 is designed to provide up to 1A output current and to operate down to 1V input-to-output differential. The dropout voltage of the device is guaranteed maximum 1.3V, decreasing at lower load currents. In our design，the input voltage VIN is provided by a 9V battery. In this case, the output voltage VDD is fixed at 3.3V, which is split subsequently into multiple parts and transported to other circuit modules (the microcontroller and the wireless communication circuit).

In the RBS experimental system, wireless communication circuit is designed based on a single chip 2.4GHz transceiver nRF24L01, which is produced by Nordic Semiconductor. The transceiver consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator, a demodulator, a modulator and an enhanced shock burst protocol engine. Output power, frequency channels and protocol setup are easily programmable through a SPI interface. Its current consumption is very low, only 9.0mA at an output power of -6dBm and 12.3mA in the RX mode.

In order to program and control the nRF24L01, a Texas Instruments 16-bit microcontroller MSP430G2553 is employed in our design, as shown in Fig.5. The interface of nRF24L01 and MSP430G2553 is shown in Fig.4 and Table I.

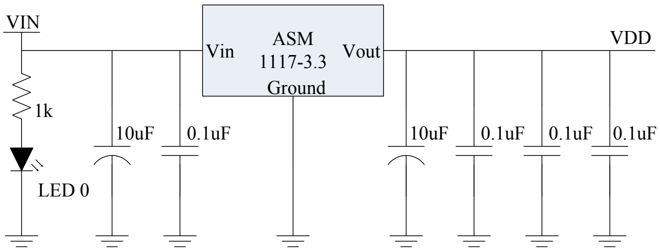


Fig. 3. Schematic of the power circuit

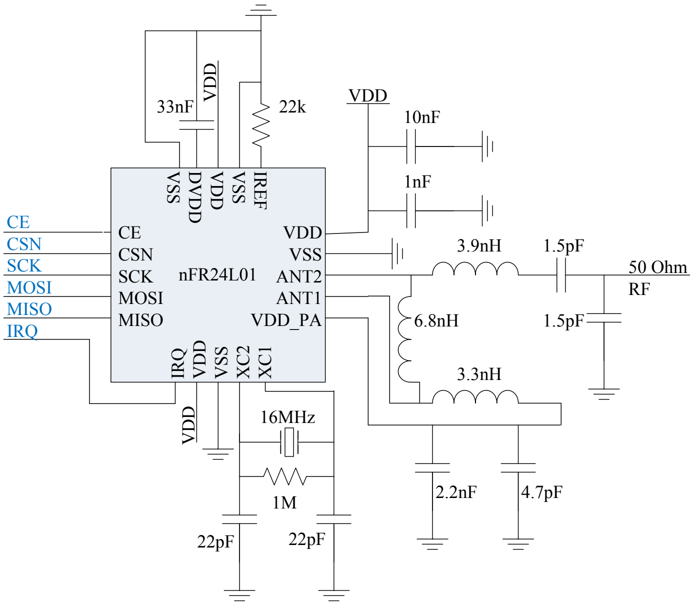


Fig. 4. Schematic of the wireless communication circuit

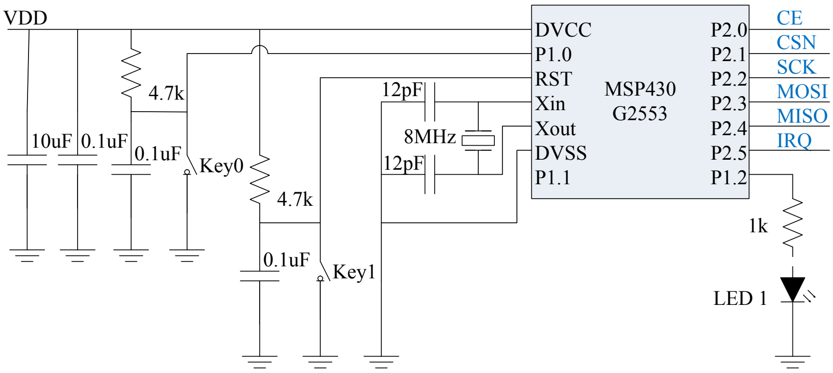


Fig. 5. Schematic of the microcontroller circuit

Table 1. Interface of nRF24L01 and MSP430G2553

Name	Pin Functon	Description
CE	Digital Input	Chip enable
IRQ	Digital Output	Maskable interrupt pin
CSN	Digital Input	SPI chip select
SCK	Digital Input	SPI clock
MOSI	Digital Input	SPI slave data input
MISO	Digital Output	SPI slave data output, with tri-state option

The CE (Chip Enable) pin is used to set the nRF24L01 into TX or RX mode. The nRF24L01 also has an active low interrupt pin (IRQ). When MSP430G2553 writes '1' to the interrupt source of nRF24L01, the IRQ pin will go inactive. The interrupt mask part of the CONFIG register in nRF24L01 is used to mask out the interrupt sources that are allowed to set the IRQ pin low. By setting one of the MASK bits high, the corresponding interrupt source will be disabled.

The SPI interface of nRF24L01 is a standard SPI interface with a maximum data rate of 10Mbps.The SPI bus is usually a high-speed serial bus that connects a master device to one or more slave devices. In our design, the MSP430G2553 is the master and the nRF24L01 is the slave. All communications are initiated by the master. The SPI protocol behaves like a ring buffer, so that whenever the master sends a byte to the slave, the slave sends a byte back to the master. The slave can use this behavior to return a status byte, a response to a previous byte, or null data (the master may choose to read the returned byte, or ignore it). The bus operates on a 4-wire interface as follows:

1. CSN (SPI Chip Select) selects which slave should listen on the bus. Many slaves can be connected to the bus (they share the other three wires), but only one can be selected to communicate at a time.
2. SCK (SPI Clock) carries the clock signal that synchronizes the master with the active slave. In our design, this wave is generated by a specified pin (P2.2) of

MSP430G2553. It determines the speed at which the SPI connection transmits data.
3. MOSI (SPI Slave Data Input) carries data bits from the MSP430G2553 to the nRF24L01.
4. MISO (SPI Slave Data Output) carries data bits from the nRF24L01 to the MSP430G2553.

In our design, the wireless communication circuit can be set up as a receiver or transmitter by the MSP430G2553. When the communication circuit works in the receiver mode, the nRF24L01 is configured as a RX mode. To enter this mode, the nRF24L01 must have the PWR_UP bit set high, PRIM_RX bit set high and the CE pin set high. In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded. When the communication circuit works in the transmitter mode, the nRF24L01 is configured as a TX mode. The TX mode is an active mode where the nRF24L01 transmits a packet. To enter this mode, the nRF24L01 must have the PWR_UP bit set high, RIM_RX bit set low, a payload in the TX FIFO and, a high pulse on the CE for more than 10μs.

Based on the system scheme and the circuit schematics mentioned above, a small-scale RBS experimental system has been developed, which contains one sender and two receivers, just as shown in Fig.6.

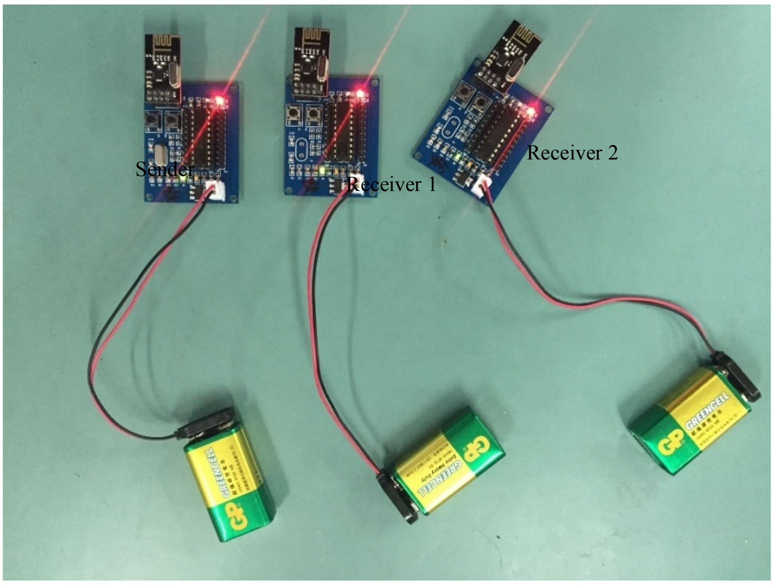
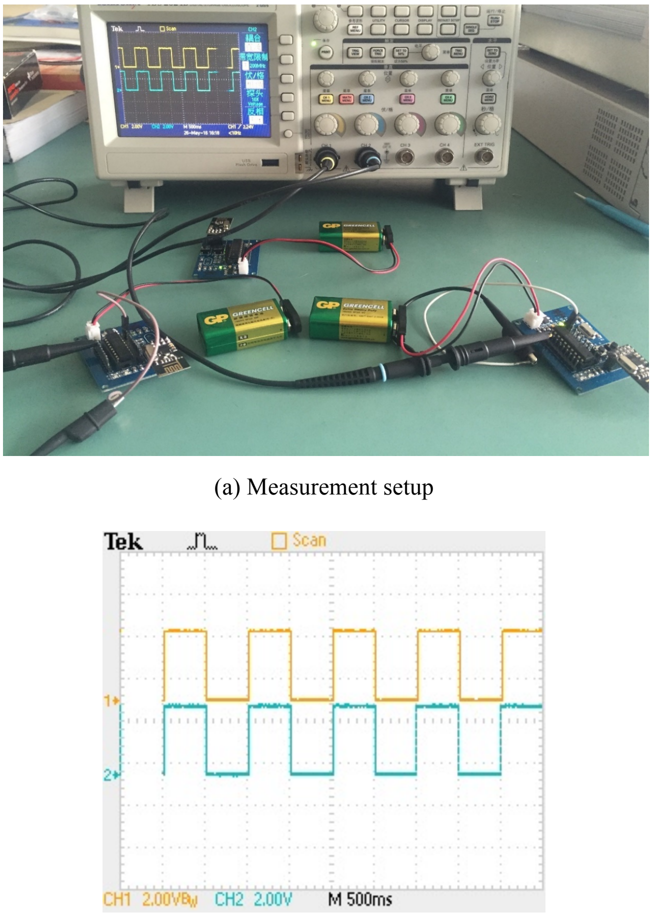


Fig. 6. Photograph of the RBS experimental system

4 Experiments

In order to make it easier to test the performance of the time synchronization experimental system, a synchronous effect indicator is designed in the microcontroller circuit. It contains a light emitting diode and a current limiting resistor, which are connected in series and fixed to the microcontroller's P1.2. Each receiver outputs a pulse-per-second signal with a duty ratio of 50% at the P1.2 pin based its local clock. So it is reasonable to assess the synchronization effect by measuring the two pulse-per-second signals use oscilloscope or time interval counter.

In order to gurantee the accuracy of the measurement, the measurement instruments usually need several hours for warm-up after turning on. In our experiment, all of the measurements were carried out four hours after the experimental system and the measurement instruments were powered on.



(a) Measurement setup

(b) Measurement result

Fig. 7. Measurement using oscilloscope TDS2024B

The Fig.7 gives the measurement result of oscilloscope TDS2024B, where we can observe both the rising or falling edges of the two pulse-per-second signals are basically the same. And by measuring the time interval between the rising edges of two pulse-per-second signals using a time interval counter, we can get more accurate measurements.

According to the real measurement result of the time interval counter FLUKE PM6681, the time synchronization error between the two receivers is about 406 microseconds, just as shown in Fig.8. The error is mainly due to the individual differences of the electronic components in the receiver. For example, the actual frequencies of the crystal oscillators in two receivers are unlikely to be exactly the same, which will cause the microcontroller's processing speed to be different. So the receivers will spend different time on the same task, even if they receive the synchronization instructions from the sender at the same time.

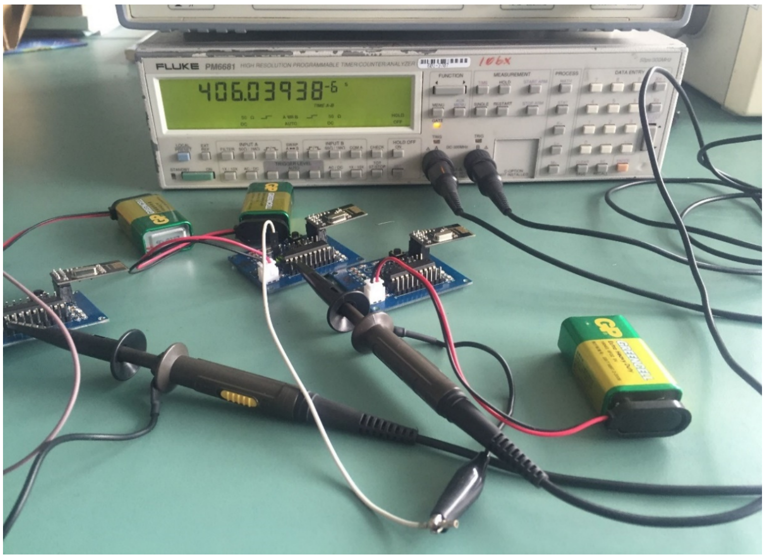


Fig. 8. Measurement using time interval counter PM6681

In addition, experiment results show that the maximum effective transmission distance of time synchronization information between the sender and the receivers is about 200m. This effective transmission distance is measured in some restrictions such as PCB printed antenna, no power amplification, 250kbps data transmission rate and open outdoor environment. In order to expand the wireless communication distance of the experimental system in complex environmen, the common practice is to select a high gain antenna and to increase the power of the transmission properly. But it will increase the power consumption of the system, and then reduce the working life of network nodes. It can be considered that searching a perfect compromise between transmission distance and power consumption is a challenging task in practical project application.

5 Conclusions

In summary, the significance of our work lies in: (1) A compact reference broadcast time synchronization experimental system based on RBS protocol is designed and implemented. (2) A variety of experimental schemes are designed to evaluate the time synchronization accuracy of the system. (3) Combing theoretic analysis and experiment, the reasons of the RBS time synchronization error are analyzed. The experimental results show that the local clocks of those nodes with a distance less than 200 meters can be adjusted synchronously with a time synchronization error less than 410 microseconds. The circuit design scheme of the time synchronization experimental system proposed in this paper may be taken as technical references for the planning and designing of low cost, miniaturization and high accuracy nodes in wireless sensor networks.

The energy limitation of nodes is one of the common features of WSN. Our main research plan in the future is to reduce the energy consumption of nodes as much as possible under the premise of ensuring the synchronization accuracy of the time synchronization algorithm. The energy saving schemes or protocols including the hardware power control, on-demand synchronization mechanism, intelligent wake-up mechanism to improve the energy efficiency in different aspects will be focused on. The verification and evaluation will be done through a series of computer simulations and practical experiments.

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