The Key Technology Design of the Real-Time Monitoring System Based on FPGA

https://doi.org/10.3991/ijoe.v15i05.8814

Bengang Bao(✉), Xiangping Zhu, Yonghong Tan
Hunan University of Science and Engineering, Yongzhou, China
bbg_762001@126.com

Abstract—Due to having a direct affect for the growth of crops, the monitor and modification for the indicators of Greenhouse environment play significant roles in improving the yield of crops. The system, which adopts FPGA technology to control and modify the air condition and lighting system by collecting and analyzing the data of the temperature and humidity, has achieved good effects in practice. In our study, the key technology of real-time data acquisition system based on FPGA is proposed. In particular, based on FPGA, the designed ADC0809 and asynchronous FIFO can save the data in real time, which can be analyzed and disposed timely, so that the environment can be corrected in time..

Keywords—Data acquisition, FPGA, ADC0809, Asynchronism FIFO

1 Introduction

With From With the development and popularization of computer technology, the data acquisition system has been rapidly applied in many fields. Now it plays an important role in such areas as industrial control, intelligent agricultural production, military electronic equipment and medical monitoring. In the process of production, the application of this system can collect, monitor and record the production parameters on the spot, which provides information and means in return in order to improve the quality of products and lower the costs. [3]. [5]. How to improve the yield and survival rate of greenhouse crops has been a very concerned issue as greenhouse crops have made outstanding contributions to the improvement of human's life. The environmental parameter is one of the most important factors that affect the yield and survival rate of greenhouse crops and hence how to design a suitable environment for crop growth has become a key problem. It is necessary to monitor and control the real-time environmental changes to design a suitable environment. With the development and popularization of computer technology, the data acquisition system has been rapidly applied in many fields. Now it plays an important role in such areas as industrial control, intelligent agricultural production, military electronic equipment and medical monitoring.

In the process of crop growth, the data acquisition system can be used to collect, monitor and record the environmental index of the greenhouse in order to improve the crop yield and lower the costs. The application of FPGA to data acquisition can obtain

a lot of dynamic information. It is a powerful tool to analyze the instantaneous physical process. FPGA has the rich I/O port, programmable gate array and soft core. Several of ports can input and output in parallel, so that data can be parallel processing, and processing speed is fast. Moreover, greenhouse environment real-time monitoring system based on FPGA meets many function control requirements, such as multipoint gathering for temperature, humidity and illumination information, and real time data analysis and processing. Specifically, the task of data acquisition system is to collect the analog signal from the sensor and convert it into digital signal which can be recognized and addressed by the computer, calculate and process the signal correspondingly according to different needs and get the required data. Meanwhile, the data acquisition system can print or display the data obtained by the computer in order to monitor particular physical quantities. Some of the data will also be used by the computer control system to control specific physical quantities. On the one hand, this monitoring system adopts FPGA technology to realize the real-time collection and analysis of the temperature and humidity of the environment; on the other hand it can control the air-conditioning system and adjust lighting system in the greenhouse, all of which have achieved good results in practice.

This paper is organized as follows. In Sect. 2, overall system design is proposed. In Sec.3, the top-level circuit design of FPGA is addressed. In Sec.4, bottom module circuit design of FPGA is discussed. Finally, the conclusions are given in Sect. 5.

2 Overall System Design

The environment of greenhouse is featured by high humidity, high acidity, little infrastructure, numerous crops with dynamic changes. Through investigation and analysis, the greenhouse monitoring system demands of real-time collection of atmospheric temperature and humidity, soil temperature and humidity, the intensity of sunlight and the concentration of CO2. By using FPGA as the control chip to design the data acquisition system, it shows good real-time and modifiability, and can be helpful to upgrade and add functions of the system, combining with the characteristics and requirements of the greenhouse monitoring system. The system block diagram of data acquisition part such as Fig. 1

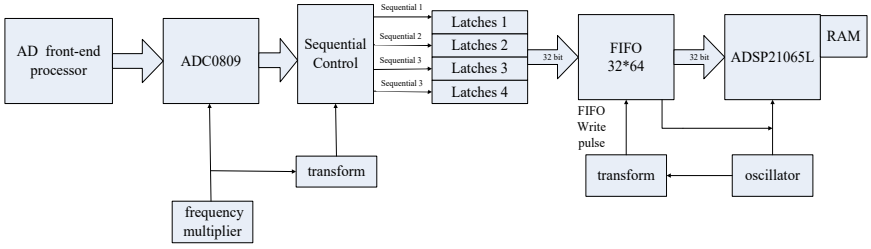

Fig. 1. Block diagram of data acquisition

3 Top-level Circuit Design of FPGA

This design which comprises of a high-speed data acquisition system and its processing part with a 32x16bit storage spaces, is a small high speed data acquisition and real time processing system that integrates data acquisition, data storage and processing. It is composed of ADC chip ADC0809, FPGA chip EPF10K10TC144-4 and peripheral circuit. [1]. [2]. [7]. the whole FPGA circuit module incorporates the A / D conversion circuit, trigger circuit, sequential circuit, control circuit and buffer circuit FIFO, see Fig. 2.

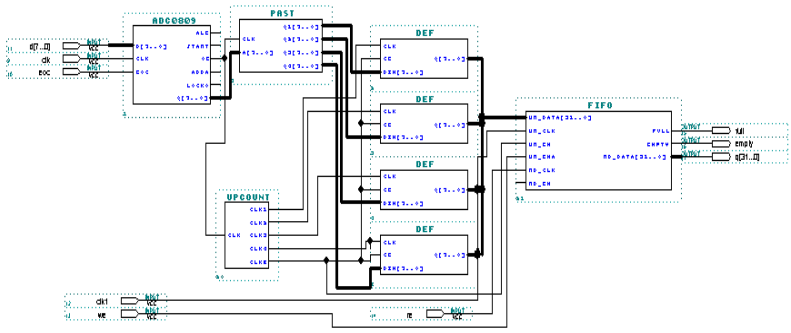

Fig. 2. Top-level circuit design of FPGA

In Fig.3, the data needs to be collected is transmitted to the ADC0809, then the data q [O7.0] converted by A / D is output from the ADC0809 port. Next, the converted data enters the data allocator, whose clock clk links the OE signal of the ADC0809. The data allocator outputs data q1 with its first rising edge and stores data q1 into the latch 1. Afterwards, the data allocator stores data into the latch 2 with its second rising edge and so on. The control clock of the latch is generated by a clock control module, up count, which takes the output OE of ADC0809 as the control end to produce five different clock signals. Those fives signals that are used as the control clock of four latches and the write-enable control signals of FIFO, make the data accessed by the data distributor and latch more accurate and complete. Under the control of the clock, data in the four latches are merged into 32-bit data and cached together into a 16*32-bit asynchronous FIFO. The write-enable signal of the FIFO is controlled by the output OE of the ADC0809. The data controlled by Verilog language is stored in the position determined by the written address in the FIFO, and the corresponding change of the written address takes place. When the space of FIFO is full, the output terminal full will notify the following digital signal processing system, which controls the read enable signal of the FIFO to take effect. The data in the FIFO will then be read according to the corresponding read address. When all the data in the FIFO has been read out and the empty signal is valid, the digital signal processing system will stop reading the data. The simulation waveform of this overall system program is shown in Fig.3.

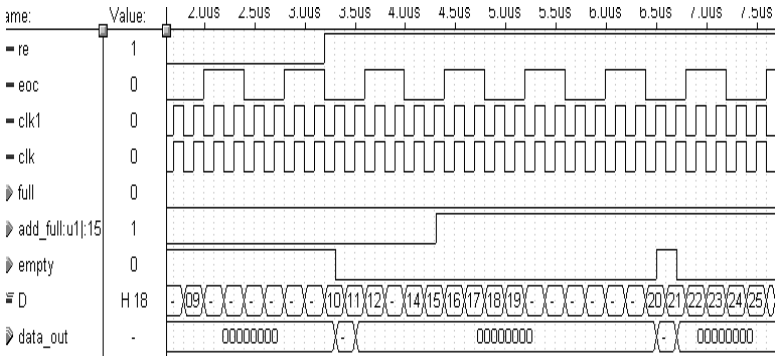

Fig. 3. The simulation waveform of this overall system program

4 Bottom Module Circuit Design of FPGA

4.1 Control Module Design for ADC0809 Chip

The working process of ADC0809 in the system is as follows: the data collected from outside is transmitted from D [7.0] into ADC0809, controlled by the clk clock to convert ADC data and output Q. [7.0] into the link below the system. The output control end OE is the clock control signal of the following links, whose simulation waveform is shown in Fig .4.

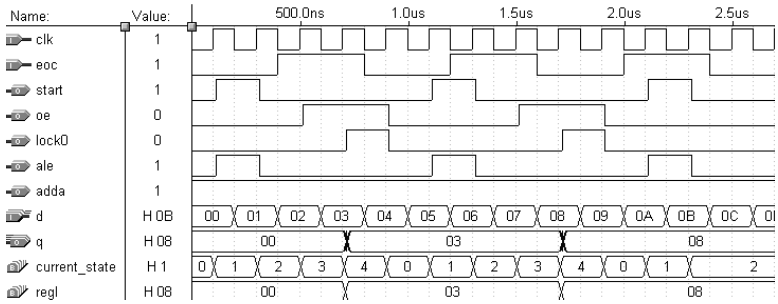

Fig. 4. Simulation waveform Control Module Design for ADC0809 Chip

The fAs can be seen from Fig.4, the data continues to enter the ADC0809. It is converted and stored in the latch within the ADC0809. The eoc becomes low level after completion of conversion, while the data is output only if OE is high level. The output data shown in the diagram is only the data corresponding to OE when it is valid. The rest of the data is replace Data allocation module designed by the new data after conversion.

4.2 The design of Data Allocation module

To the electrical model of the data allocation module is shown in Fig.5.

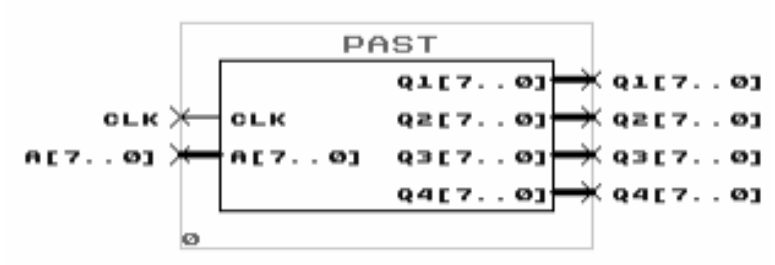

Fig. 5. The design of data allocation module.

The function of the data allocator in the system is to convert the data outputted from the ADC0809 at different clock rise edge, according to the control of the clock, so that the data can be stored in different latches. As the first rising edge of clk comes, it outputs A. [7...0] from Q1 terminal, and Q2 terminal when the second rising edge appears, and so forth. The clk is controlled by the OE of ADC0809 and the rising edge of OE indicates that the data is outputted from ADC0809. The simulation waveform is shown in Fig.6.

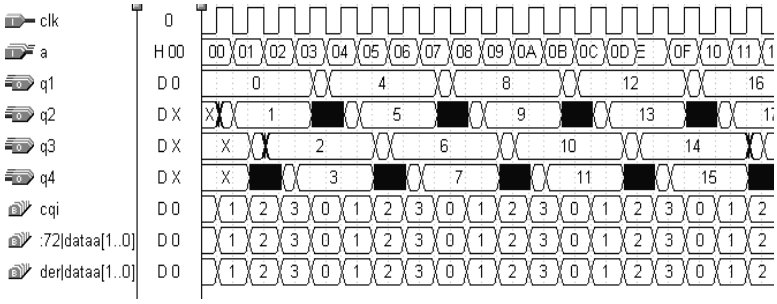

Fig. 6. Simulation waveform of data allocation module

4.3 Lock Module Design

The electrical model of the latch is shown in Fig.7.

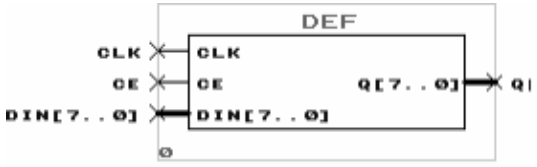

Fig. 7. Lock Module Design

The role of latch in the system is to convert the output data of ADC0809 to latch, aiming to avoid the data loss caused by the continuous write data beyond the FIFO's capacity. It is also controlled by the ADC0809's OE output after the clock conversion. When the rising edge comes, the data is stored in the latch. When the output control side ce is high level, the outputted data enters into the FIFO. The simulation waveform is shown in Fig.8.

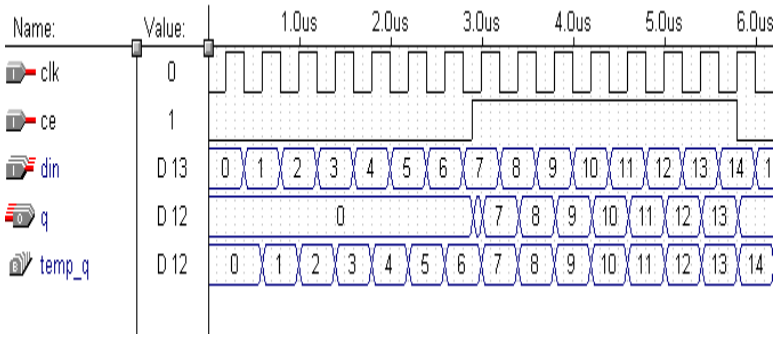

Fig. 8. Simulation waveform of Lock

4.4 Design of clock conversion module

The electrical model of the clock conversion module is shown in Fig.9.

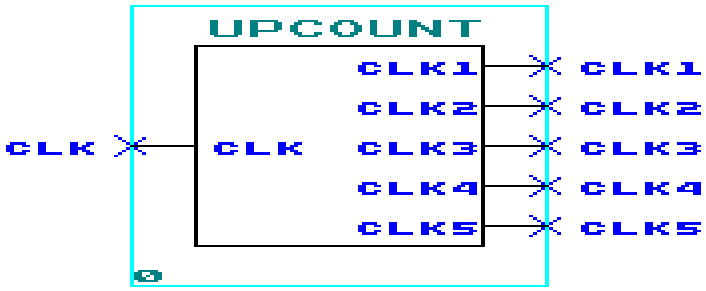

Fig. 9. Design of clock conversion module.

The function of the system in the clock conversion module is to produce the clock of the data distribution module and latch and the write enable signal of the FIFO, which is input from the OE output of the ADC0809 and is counted by the way of counting. When the first rising edge arrives, clk1 generates a single period high level in the same period, while the other time is a low level state; when the second rising edge arrives, clk2 generates a period of high level state, but only maintains one cycle. Other times are low levels. And so on. This enables the data distributor and latch to accurately gating and latching data without causing confusion or loss of data storage. The simulation waveform is shown in Fig.10.

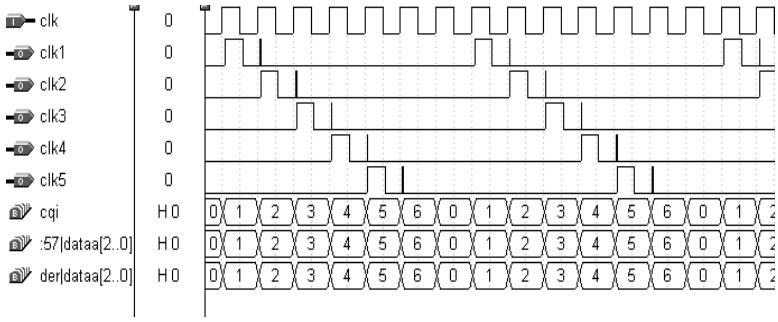

Fig. 10. Simulation waveform of clock conversion module

As shown in Fig.10, according to CLK, five different clocks are generated. And those four latches have their own control clock from clk1 to clk4 respectively. When the arrival of the rising edge, data outputted from the data distribution module is latched; when CLK is low level, the latch is no longer access to other data to make sure accuracy and orderliness of the latched data. For the data outputted from data distribution module has some glitches, if the clock is effective all the time, latch access to data will produce an error. When Clk5, the asynchronous FIFO write enable signal, is valid, then FIFO will latch the data into two port RAM.

4.5 FIFO module circuit design

FIFO, the abbreviation of First in First Out, is a kind of first in and first out data buffer. It can only write and read the data sequentially. The data address is realized by automatically adding 1 to the inner read or write pointer. FIFO is usually implemented by using the dual port RAM and the read-write address module [8]. The electrical model of asynchronous FIFO is shown in Fig.11.

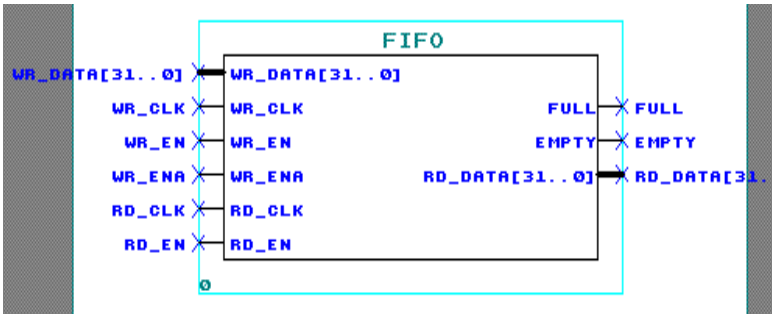

Fig. 11. FIFO module circuit design

In this system, the write enable signal and the read enable signal of asynchronous FIFO are controlled by the follow-up system. The working process is as follows: the write enable control end is set by the subsequent system as effective. Data converted by adc0809 is temporarily stored in the location specified by the written address in the

dual-port RAM under the control of the clock. If the data storage of FIFO has been fully occupied, the full signal FULL is valid, and the follow-up system will invalidate the write-enable signal so that the data will no longer be written and errors will be avoided. When the later system needs data, the read enable re becomes effective, then the data can be read out. When the data in the FIFO has been read out, the empty signal EMPTY will be valid. The subsequent system will be notified to stop reading the data in the FIFO to avoid misreading the data. The whole FIFO module includes the read-write address, the empty or full generation module and dual-port RAM modules. The simulation waveform is shown in Fig.12.

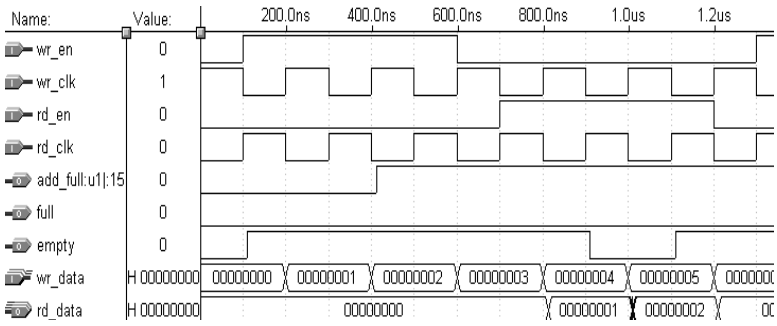

Fig. 12. Simulation waveform of FIFO

From the waveform diagram, we can see that under the control of read or write clock, the input data wr_data is "00000001" and "00000002" when the write enable signal wr_en is high level. So when the write enable signal is at a high level, the data read out is also "00000001" and "00000002".

5 Conclusion

This paper designs the monitoring system of greenhouse environment based on FPGA, hoping to realize the real time collection and analysis of the temperature and humidity of the environment, and devise a key design of the real time data acquisition system based on FPGA. The controller module, data distribution module, clock conversion module and asynchronous FIFO module of ADC0809 which are programmed by verilog language has obtained a good simulation waveform in Quartus Ⅱ. The top-level design of real-time data acquisition system in real-time monitoring system based on FPGA compiled by verilog language obtained good experimental results when download to the FLEX series chip EPF10K20RC208-3.

6 References

[1] L. Q. Z, B.Z. Guo, X. L. Y, et al. Design of high-speed data acquisition system based on FPGA[J]. Applied Mechanics & Materials 457(2013)878-882.

[2] J. Liu Design of a dual channel high-speed wideband synchronous data acquisition system[C]// IEEE International Conference on Electronic Measurement & Instruments. IEEE, (2016) 295-299.
[3] W.C. Guo, H.J. Chen. Green house Monitoring System Based on Wire Less Sensor Networks[J].Transactions of the Chinese Society for Agricultural Machinery41(2010):181-185.
[4] W. Zheng, R. Liu, M. Zhang, et al. Design of FPGA based high-speed data acquisition and real-time data processing system on J-TEXT tokamak [J]. Fusion Engineering & Design 89(2014):698-701. https://doi.org/10.1016/j.fusengdes.2014.01.027
[5] X.F. Zhao, R. Xiang Zhu. Design of environment monitoring system for refrigerated truck of agricultural products based on ARM [J]. Transducer and Microsystem Technologies 29(2010):98-100
[6] X.H. Li, Y.J. Wang. A Mountainous Orchard Data Acquisition System Based on Wireless Sensor Netwok [J].Computer Engineering 41 (2015):238-243.
[7] R. Rajpal, H. Mandaliya, J. Patel, et al. Embedded multi-channel data acquisition system on FPGA for Aditya Tokamak[J]. Fusion Engineering & Design112 (2016)964-968. https://doi.org/10.1016/j.fusengdes.2016.03.068
[8] YANG Lin-nan, LI Hong-gang. Design of High Speed Multichannel Data Cathering System Based on FPGA [J].Computer Engineering.2007, 33(7):246-248.
[9] A. Aljumah, M. A. Ahmed. Design of High Speed Data Transfer Direct Memory Access Controller for System on Chip Based Embedded Products[J]. Journal of Applied Sciences 15(2015):576. https://doi.org/10.3923/jas.2015.576.581

7 Authors

Bengang Bao works for School of Electronics and Information Engineering, Hunan University of Science and Engineering, Yongzhou, 425199, China.

Xiangping Zhu works for School of Electronics and Information Engineering, Hunan University of Science and Engineering, Yongzhou, 425199, China.

Yonghong Tan works for School of Electronics and Information Engineering, Hunan University of Science and Engineering, Yongzhou, 425199, China.

Article submitted 2018-05-03. Resubmitted 2019-01-27. Final acceptance 2019-01-29. Final version published as submitted by the authors.